Chapter IV Temperature control system

CHAPTER IV

"TEMPERATURE CONTROL SYSTEM"

4.1 Theoretical Development :

A generallised block diagram of a process control is shown in fig. 4

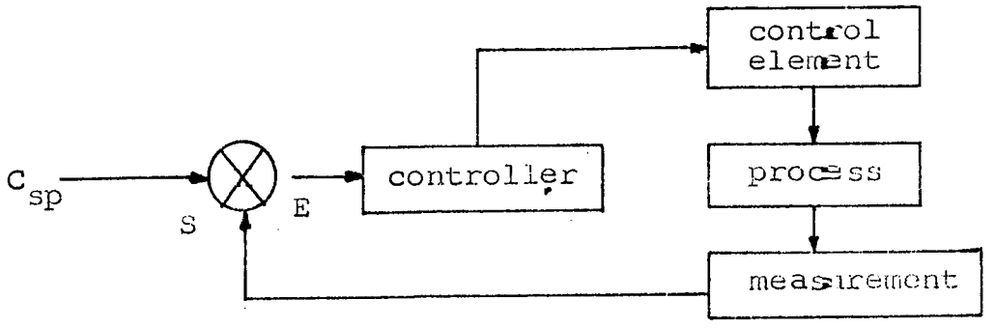


Fig. 4

C = Controlled dynamic variable.

C_{sp} = Setpoint value of controlled variable.

C_m = measured value of controlled variable.

$E = C_m - C_{sp}$ = Error signal.

The controll is exercised by

a) A comparision of the controlled variable measurement and the setpoint and

b) A determination of action required to bring the controlled variable to the setpoint value.

A computer is used as a controller. By software the control function, the setpoint and the deviation from it are defined. There are many controller modes.

4.2 A) Discontineous controller modes (1)

i) TWO position mode

This is ON - OFF type simple and cheap method used in cases were its disadvantages are tolerable.

ii) Multiposition mode : In this mode several intermediate settings of the controller output is made use of.

iii) Floaring control mode : In floating control the specific output of the controller is not uniquely determined by the error. If the error is zero the output will not change and when the error moves off the zero the controller output begins to change.

4.3 B) Contineous controller mode :

The output of the controller changes smoothly in response to the error or rate of change of error.

i) Proportional control mode :

In this mode the controller output and the error bear linear relationship. Thus over some range of errors about the set point each value of error has a nuique value of controller output in one to one correspondance. The range of error to cover the zero percentage to 100% controller output is called the proportional band. This mode can be expressed as.

$$P(t) = K_p E_p + P(0)$$

Where K_p = proportional constant between errors and controller output.

P (O) = Controller output with no error. The proportional mode introduces offset due to change in load. Hence the system is used only if the offset balance is possible.

2) Integral control mode :

This mode is called the reset action and the analytical relation describing it is,

$$\frac{dp}{dt} = K_i E_p$$

Where dp/dt = rate of controller output change.

K_i = constant, relating the rate to the error.

$\frac{1}{K_i} = T_1$ = integral time in seconds.

At any time the controller O/P is

$$P(t) = K_i \int_0^t E_p(t) + P(0)$$

Where P (O) = controller O/P at t = 0

Thus the cstate of the present controller O/P is a function of the history of errors from the time observations started at t = 0. Hence if the error doubles, the rate of change of controller O/P also doubles. If K_i is large even a small change in E_p causes large change in $\frac{dp}{dt}$. This is

shown in Fig. 4.1. This method produces destabilising effect in the close loop systems and loop response time may be increase.

3) Derivative control mode :

This mode provides that the controller output depends on the rate of change of rerror. This mode is also known as rate of anticipatory control. The analytic expression is,

$$P = K_d \, dE_p /dt + P(0).$$

Where K_d = derivative gain constant.

dE_p /dt = rate of change of error.

$P(0)$ = output with no error rate.

The derivative gain constant is also known as the rate of derivative time and is commonly expressed in minutes. For a given rate of change of error, there is a unique value of controller output. It can be noticed From fig. 4.2 that the extent of controller output depends upon the rate at which this error is changed and not on the value of the error.

The derivative mode improves the response of the close loop system. It is effective only during the transient.

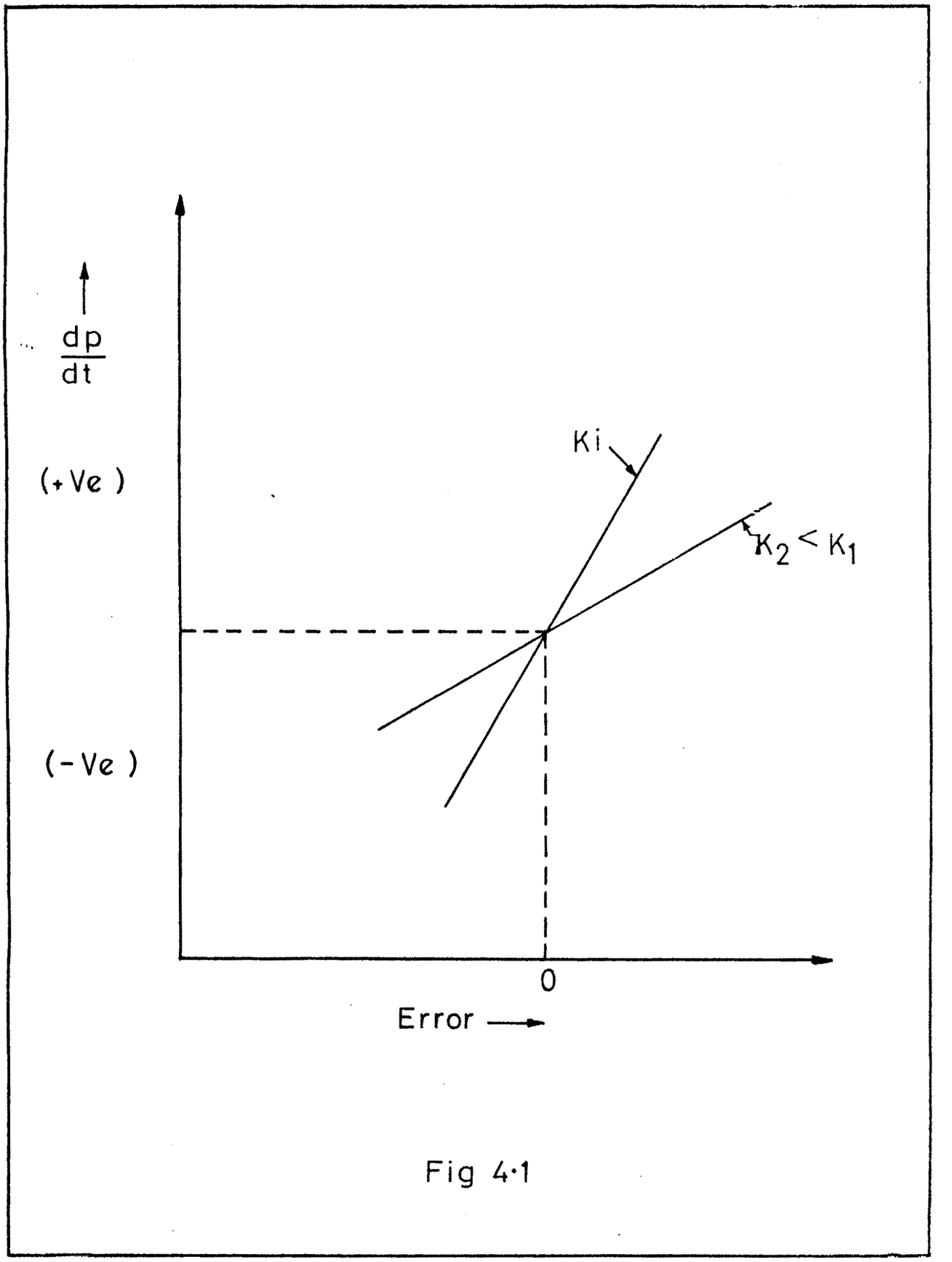


Fig 4·1

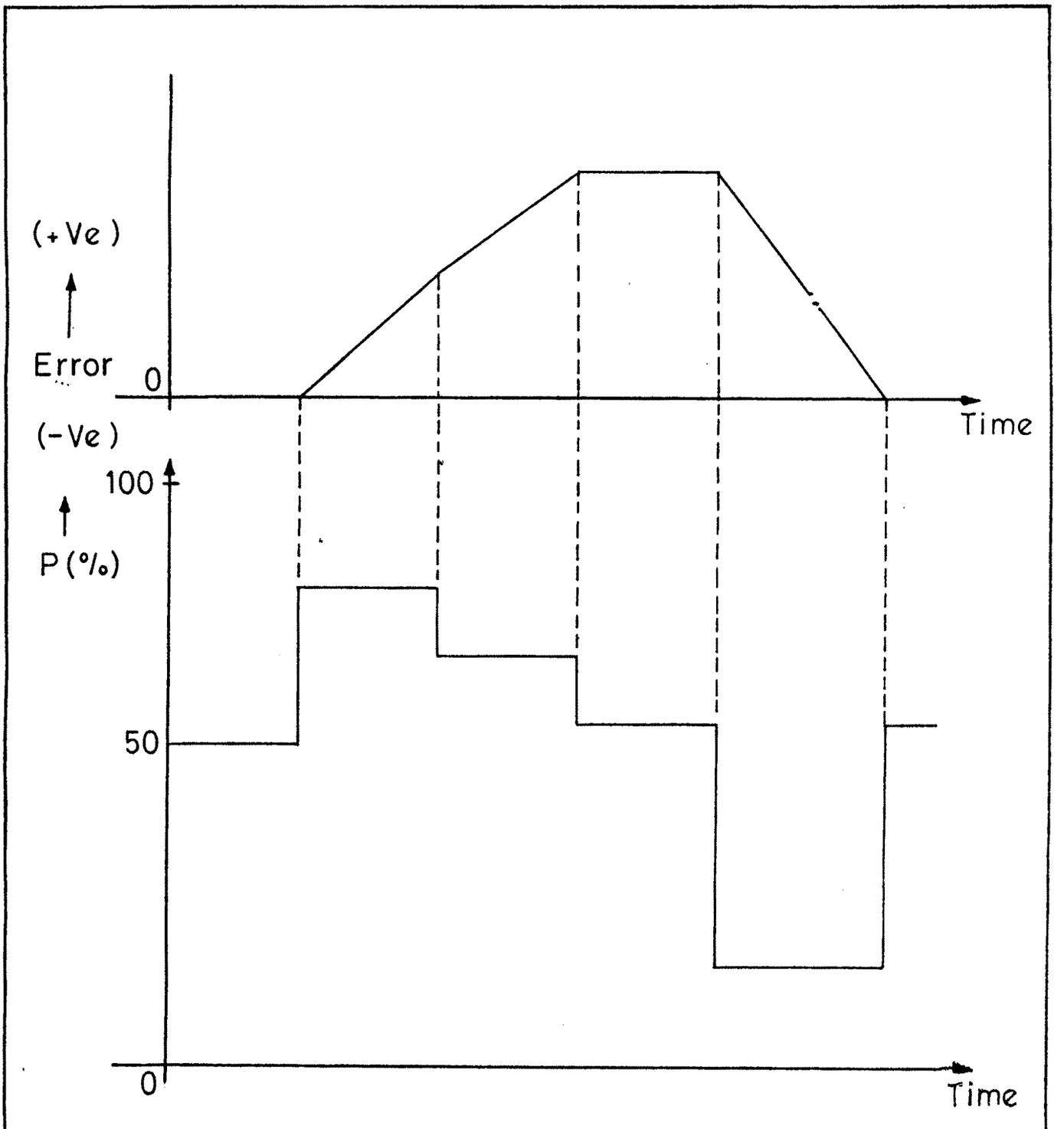


Fig. 4·2

C) Composite control mode : Integral or derivative mode alone is never used but basic modes are combined to have the advantage of eliminating the limitations of individual modes.

1) Proportional integral mode (PI) :

This mode is a combination of proportional mode and integral mode. The analytical expression for this control mode is,

$$P(t) = K_p E_p + K_p K_i \int E_p dt + P(0)$$

The main advantage of this mode is one-to-one correspondance of the proportional mode is available and the integral mode eliminates the inherent offset. Notice that the proportional gain, by design, also changes the net integration mode gain, but that the integration gain K_i can be independently adjusted. The integral function provides the required new controller output, thereby nullifying the error caused in proportional mode due to load change. The integral feature effectively provides the reset of operating point when a load change occures. The controller output is provided through a some of proportional plus integral action, which finally leaves the error at zero.

This mode is used in systems with large load changes. The disadvantage of this mode is that large overshoot is observed before setting to the operation point to minimize this overshoot the load change must be slow.

This controller mode is implemented in our system through software. Since system time constant is large, over shoot can be minimized.

2) Proportional - Derivative mode (PD) :

This is a control mode that results from a combination of the proportional mode and the derivative mode. The analytic expression for this control process is,

$$P(t) = K_p E_p + K_p K_d \, dE_p/dt + P(0).$$

The process can handle fast process load changes as long as the load change offset error is acceptiable. However, the system cant eliminate the offset of proportional controllers.

3) Proportional-Integral-Derivative (PID) :

The PID control algorithm is the universly accepted control strategy used in analog controllers. The controller output is the sum of the three seperate terms, proportional, integral or reset and derivative or rate. These terms are as shown below in fig. 4.3

The constant of proportionality K_p is called the controller gain. It is adjustable over a wide range from 0.1 to 100 in most controllers. Controller are calibrated in terms of the proportional band Pb, which is expressed as percentage.

$$Pb = 100/K_b\%$$

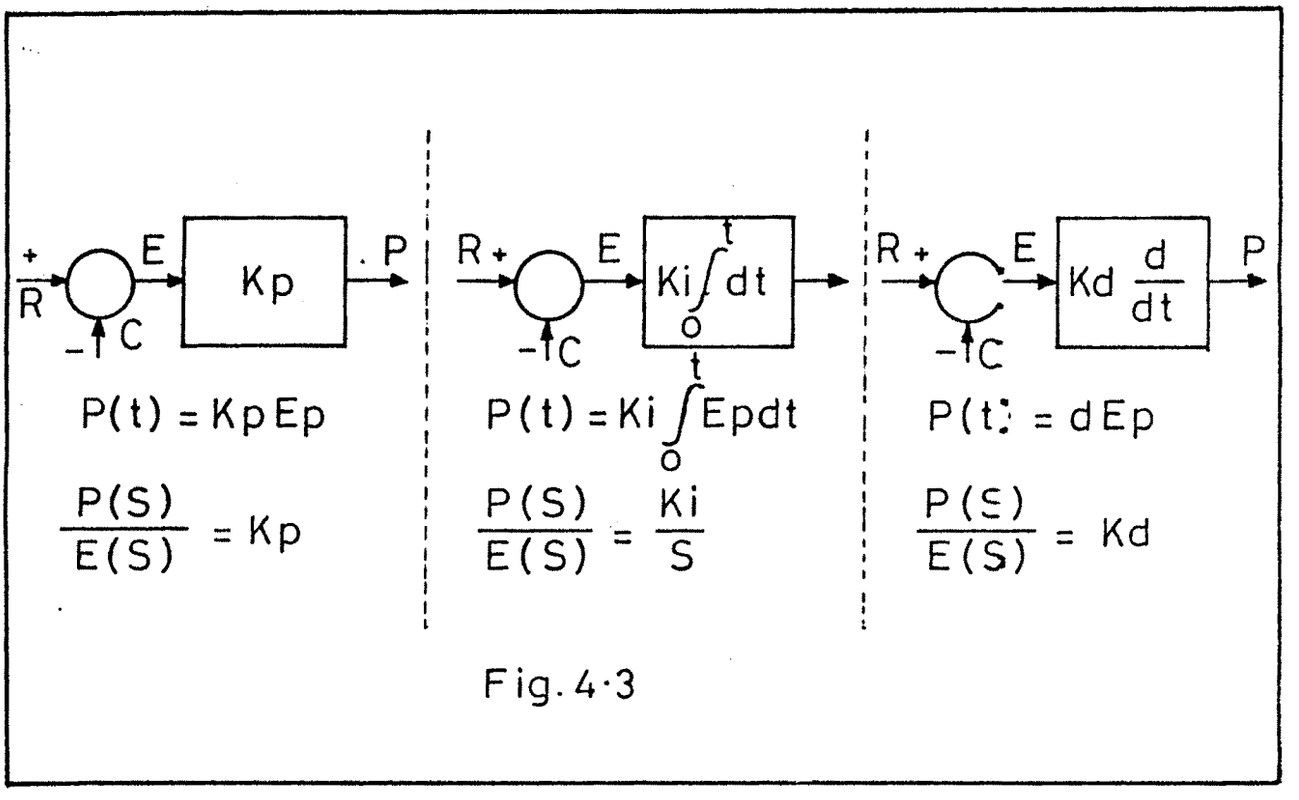

+
R
E
Kp
P
-C
P(t) = KpEp
P(S)/E(S) = Kp
R +
E
Ki ∫ dt
t
o
-C
P(t) = Ki ∫ Epdt
t
o
P(S)/E(S) = Ki/S
R +
E
Kd d/dt
P
-C
P(t) = dEp
P(S)/E(S) = Kd

Fig. 4·3

With proportional control, a permanent steady state offset between the setpoint (reference pt) and the process output variable is obtained. Addition of the integral term provides zero steady state offset under all setpoint and disturbance conditions. The integral term is almost always used with the proportional term, making a P.I. controller is described by

$$P(t) = K_p E_p + K_p K_i \int_0^t E_p dt + P(0).$$

The constant $\frac{1}{K_i}$ is called the integral time. The typical range is 0.02 to 50 minute. The addition of integral action produces a destabilizing effect in the closed loop system and the loop response time may increase. The derivative (rate control) term is used for improving the response of the closed loop system. The derivative control is anticipatory and is effective only during the transient period. The derivative control is never used alone and seldom with only the proportional control. When the derivative term is added to a PI controller the complete three term PID control algorithm is obtained.

$$M(t) = K_p E_p + K_p K_i \int_0^t E_p dt + K_p K_d \frac{dE_p}{dt} + P(0).$$

Where K_d is derivative gain constant.

When the derivative control is used in a process whose measured variable is noisy additional filtering may

be required to eliminate the effect of noise. Hence the derivative control is not used as widely as right be expected. Additionally, three term controllers are more difficult to adjust (tune) properly as compared to two term PI controllers.

4.4 Temperature control system :

In chapter - 2, we have given the characteristics of the silicon diode used as the temperature sensor. We have calculated the rate of drop of the diode forward voltage to be 2mv/oC In the temperature control system two diodes have been used so that the rate of drop of the forward voltage is 4mv/^{o}C rise of temperature. This sensor is immersed in the liquid whose temperature is to be controlled. The signal from this sensor is amplified by operational amplifier LM 308. The offset is balanced by 4-7K pot and the gain of the amplifier is adjusted by 5K pot.

About LM 308 (6)

It is a precision operational-amplifier. It has low input current and extremely low offset voltage. The features are,

1) Offset voltage guranteed less than 0.5mv.
2) maximum input bias current of 3nA over temperature.
3) offset current is less than 400 PA over temperature.
4) Supply current of only 300 MA, Even in saturation.
5) Guranteed 5 MV/^{o}C drift.

The gain and the offset of the amplifier are calibrated so that the output is zero (0) with the sensor in ice and in the boiling water. This analog equivalent voltage of the temperature is converted in to digital equivalent by ADC. This digital voltage is displayed and also processed by the microprocessor 8085 based system, we have designed. Using 8155 (A) as I/O. This digital equivalent of the temperature is inputed through port A to the microprocessor by using a software routine. The BCD output is converted in to the binary. The setpoint corresponding to the temperature 61°C is stored in the EPROM 2732. This setpoint is compared with the sensor output and the error signal is calculated. This resulting error is processed by PI software and is used to control the ON time of the heater control circuit. If the error is large the ON time is also kept large and vice versa. After every 2.5 second the program is called and the temperature regulation is done. This system can be extended for the measurement and the control of various temperature by change of the setpoint.

In fig. 4.4 the block diagram the temperature control system is shown. The heating element is energized with the help of triac and its control circuit. Actual heater control circuit and its block diagram are shown in fig. 4.5. IC 555 is used in Astable mode whose set-reset pin No.4 is controlled by the microprocessor through the

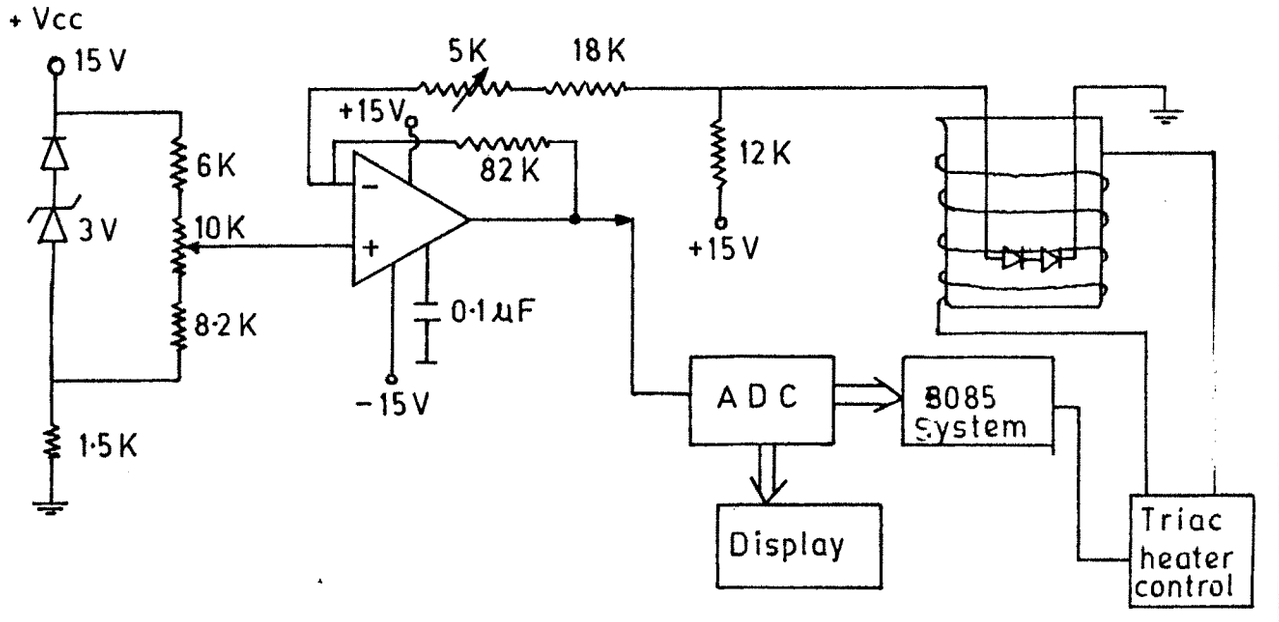


Fig. 4·4 TEMPERATURE CONTROL SYSTEM

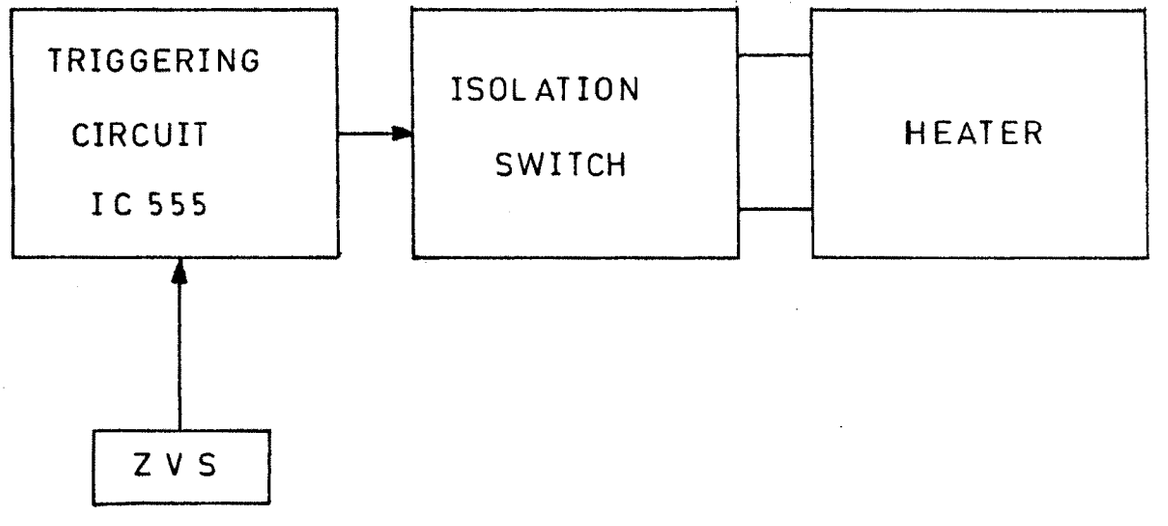
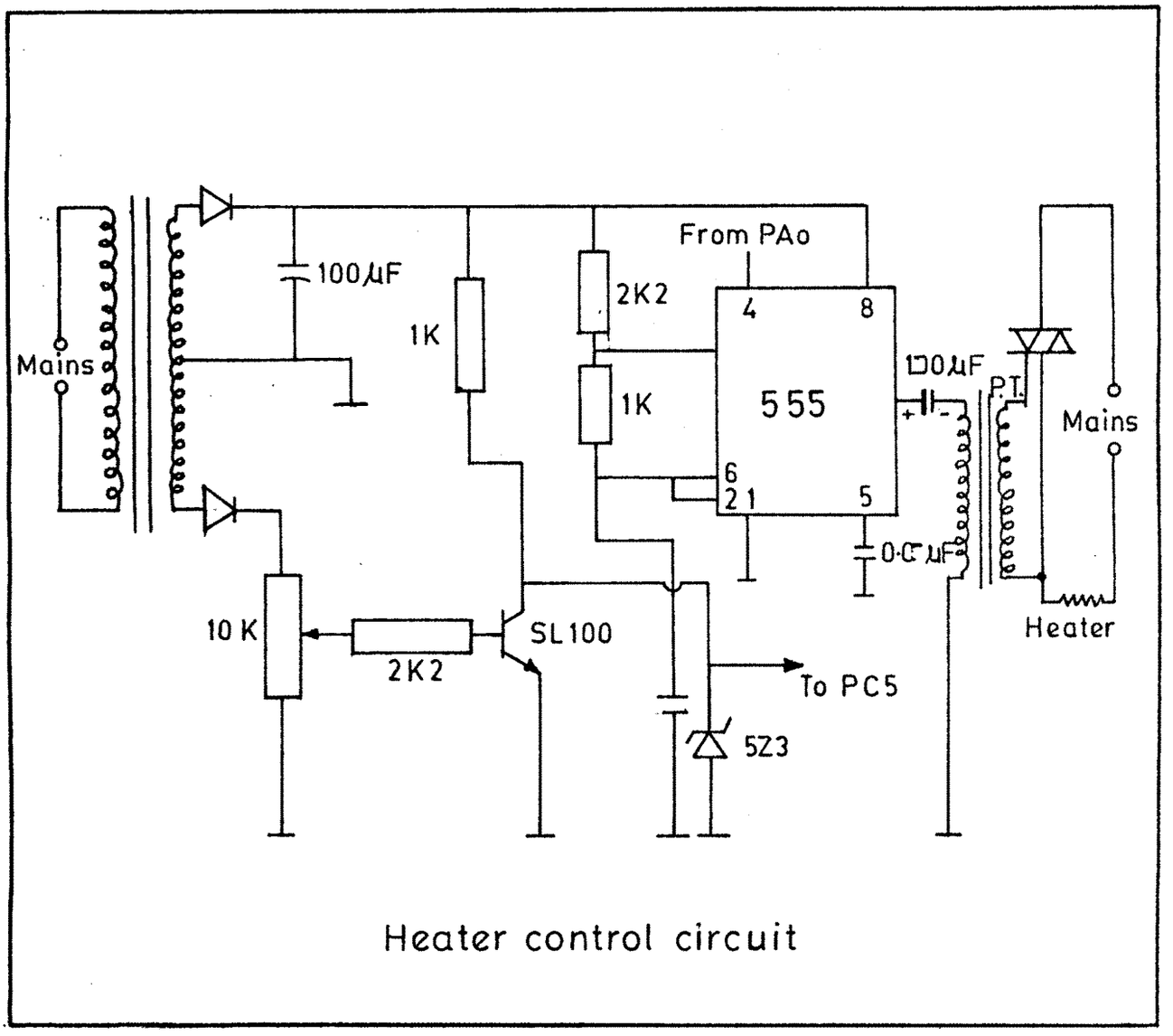


Fig. 4·5 BLOCK DIAGRAM OF HEATER CONTROL CIRCUIT.



Heater control circuit

port of 8155. This setting and resetting controls the ON-OFF time and ultimately the temperature. This triggering circuit is isolated from the power circuit by the pulse transformer. In order to avoid RFI the triac is triggered at the zero volt point of the mains voltage. The frequency of the pulse is 2KHZ. When the pin-4 is at logic high the output is enabled otherwise it is disabled.

The pulse transformed 1:1 ratio is used to isolate the trigger circuit from the power circuit. Opto-isolators are recommended for the high power control, (2).

The zero voltage switching is necessary because

i) It does not produce electrical noise.

ii) There is no need for RFI filter in the circuit.

iii) The rate of rise of voltage and the current are limited therefore the triac with low dv/dt and dI/dt rating can be used. The triac is triggered by (+ve) gate pulses at the pin-3 of IC 555 the details of the heater are described in chapter 2.

4.5 Microprocessor based system : In fig. 4.6 the minimum system around the microprocessor 8085 is shown. Here 8155-A and 8155-B are used as I/O port scratchpad, 8212 is used as a latch and 74139 is used as 2 to 4 address decoder. The EPROM 2732 is used to store the temperature controller program.

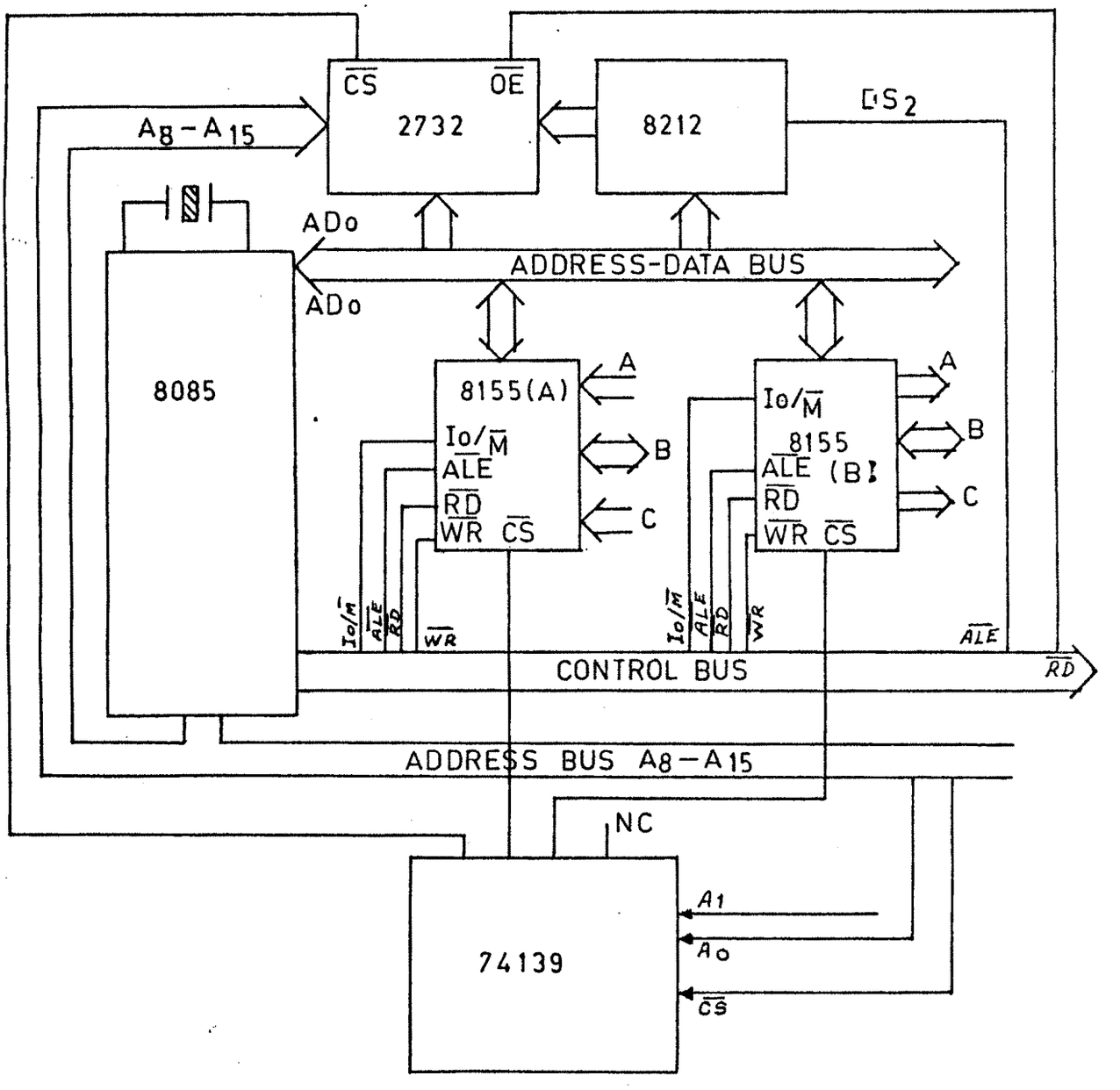

CS
OE
2732
8212
DS2
A8 – A15
AD0
ADDRESS-DATA BUS
AD0
8085
8155(A)
A
B
C
IO/M
ALE
RD
WR
CS
8155
ALE (B)
CONTROL BUS
ADDRESS BUS A8 – A15
NC
74139
A1
A0
CS

Fig. 4·6

The address decoding by 74139 for the different chips are as follows. 74139 is selected by A_{15} while A_{14} and A_{13} are used to select one of the three chips as shown below.

A_{15}	A_{14}	A_{13}	Chip selected
0	0	0	2732
0	0	1	8155 (B)
0	1	1	8155 (A)

The latch 8212 is used to demultiplex AD_0- AD_7 bus. The $\overline{ALE}$ signal is used to latch the address for 2732 EPROM. The following are the address used.

8155 (A) - RAM - 6000 to 60 FF

8155 (B) - RAM - 2000 to 20 FF

2732 - EPROM- 1000 to 1 FFF

The $\overline{ALE}$ signal is issued by the microprocessor latches, the address in 8155 and 8212 latch. In chapter-3 the details of the control signals are given.

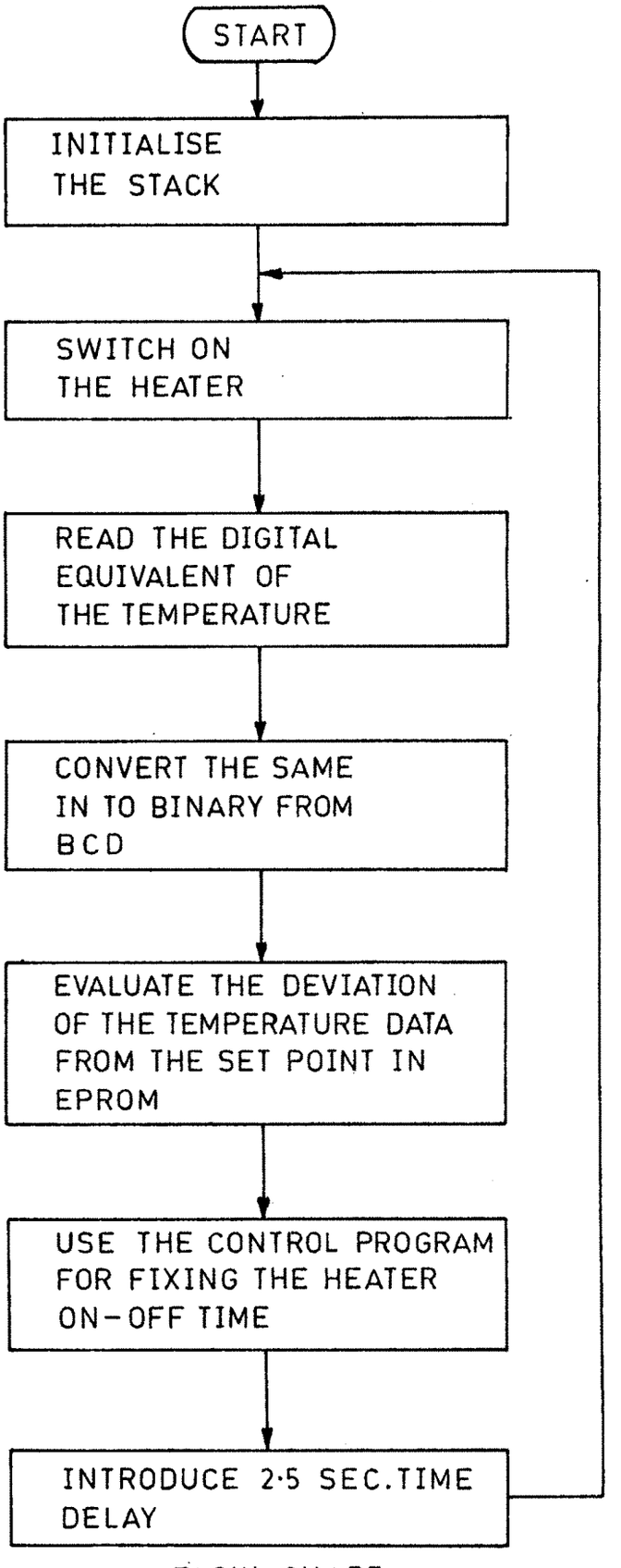
4.6 Analog to digital converter :

The ADC MC 14433 used is a high performance, low power $3\frac{1}{2}$ digit ADC having very few external component (2 resistors and 2 capacitors). The full scale range of ADC is from 1.999 V 199.9 mV. The accuracy is $\pm$ 0.05% of reading and the speed is 25 conversions/second. We have used it in full scale range of 0 to 1.999 V. It is used to

operate with LED display. The ADC also has facility to refresh multiplexed display. Output of converter is in multiplexed BCD form. Q_0 to Q_3 are data outputs and DS_1 through DS_4 are data strobe outputs. A data strobe output goes high when the data for the digit is on the Q_0 to Q_3.

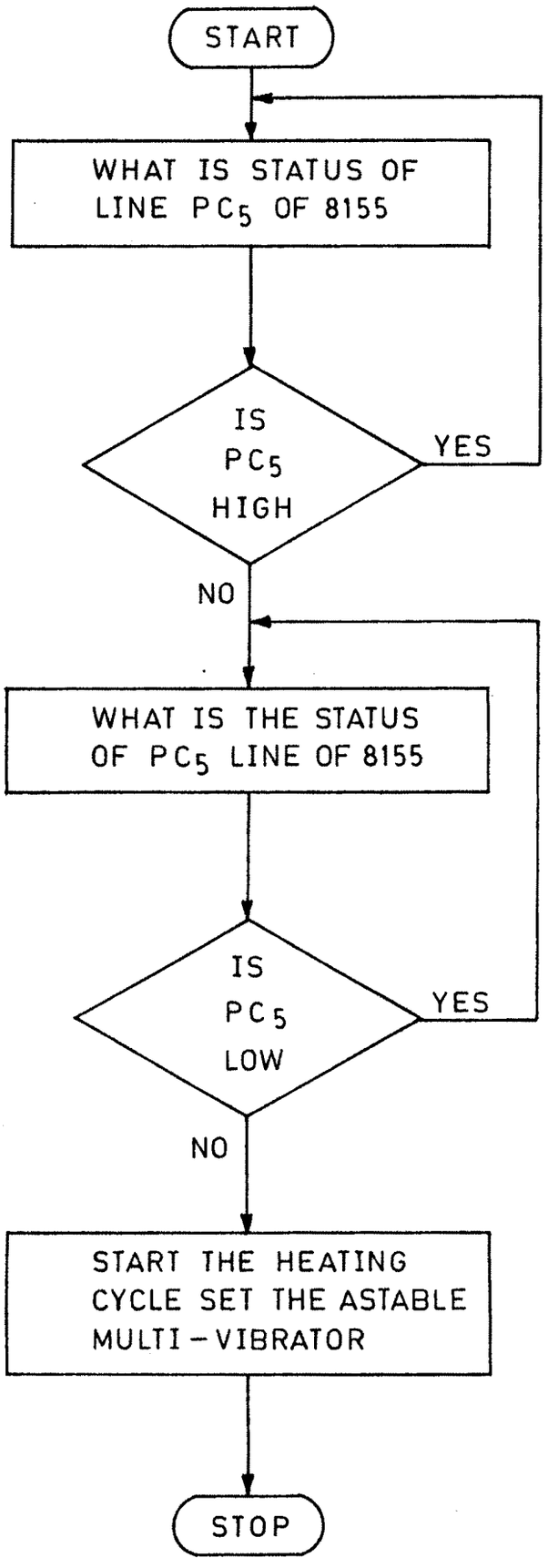
4.7 Display and driving circuit :

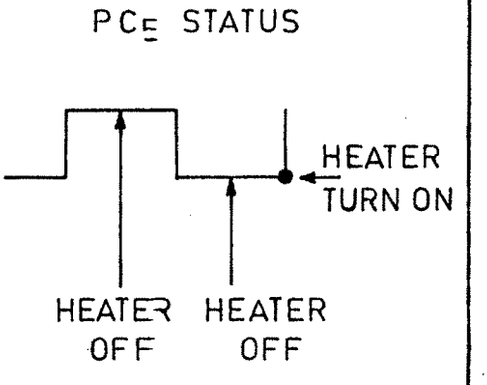
The display unit consists of 4 seven segment LED, which are common anode type. 7447 is used to convert the BCD output of ADC to seven segment with the use of multiplexed display only one BCD to seven segment converter is required. These displays are selected by SL 100 transistors. The display refreshing frequency used is 800 HZ.



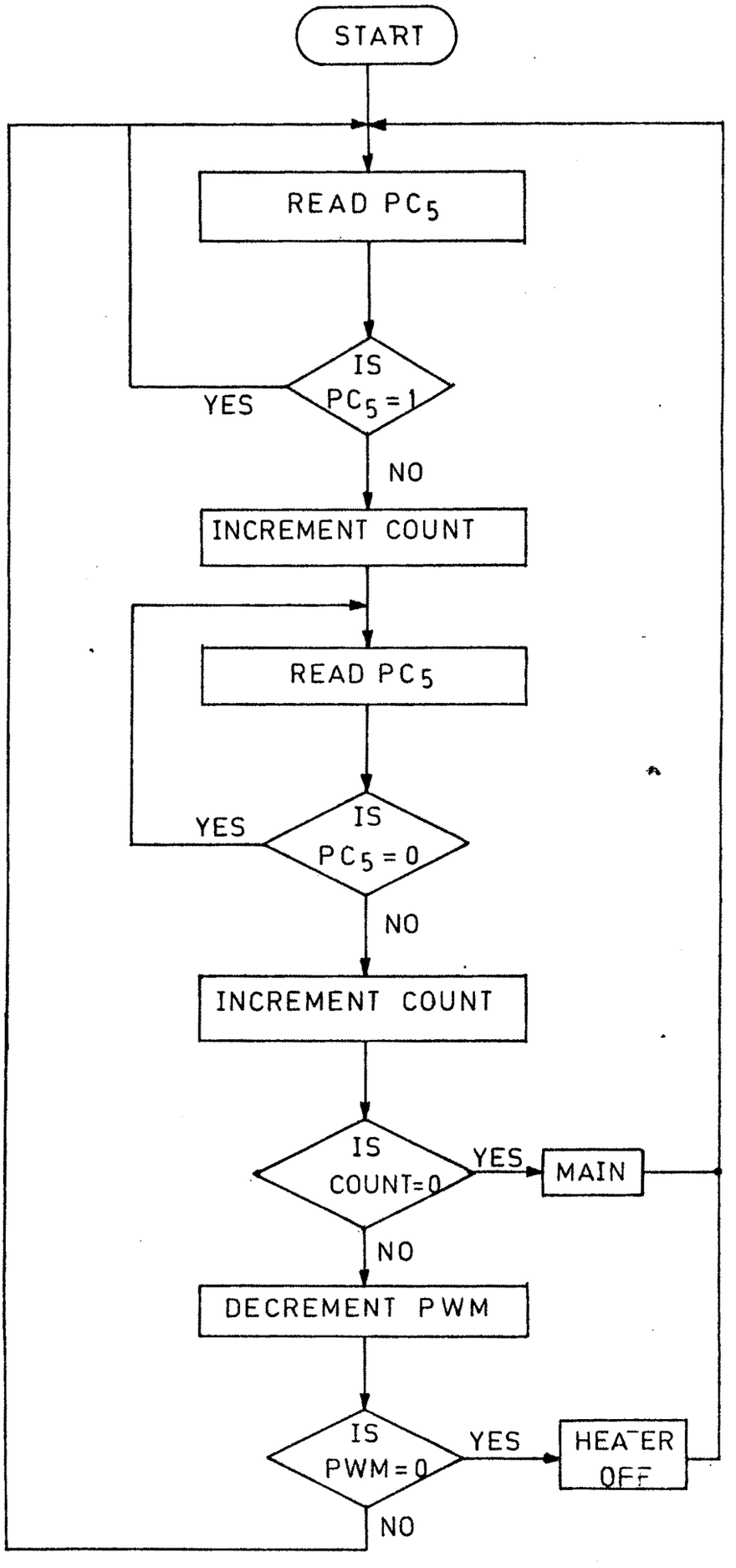
FLOW CHART

PROGRAM FOR CONTROL OF TEMPERATURE.

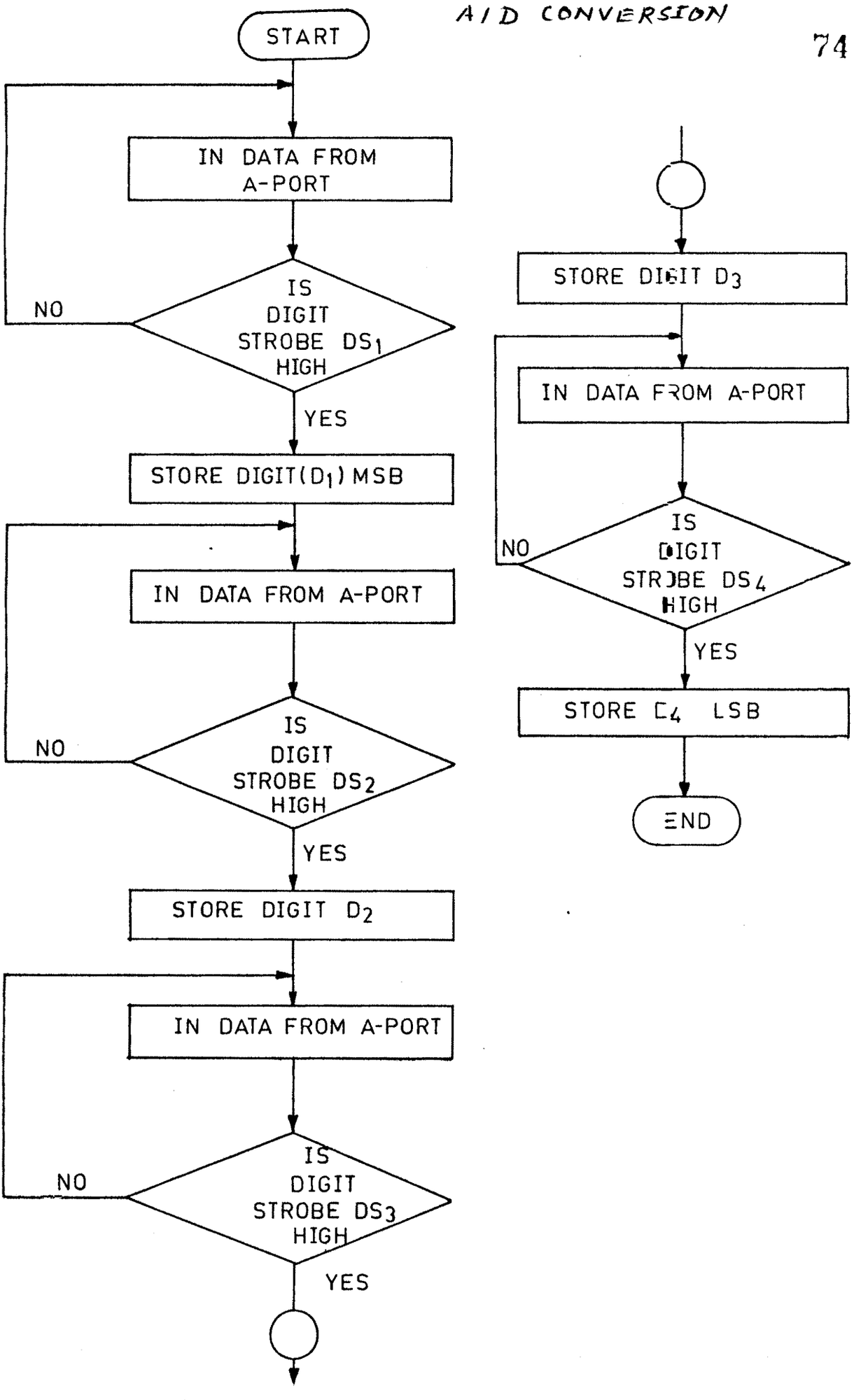


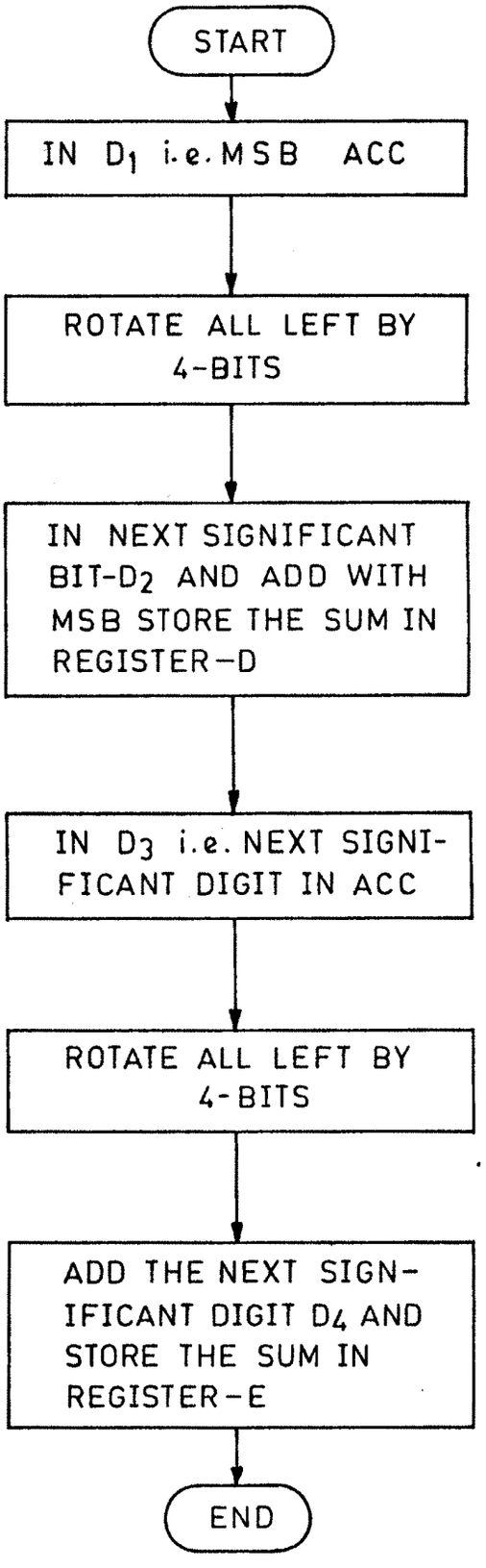


TO TURN ON TRIAC AT THE ZERO VOLT OF THE MAINS.

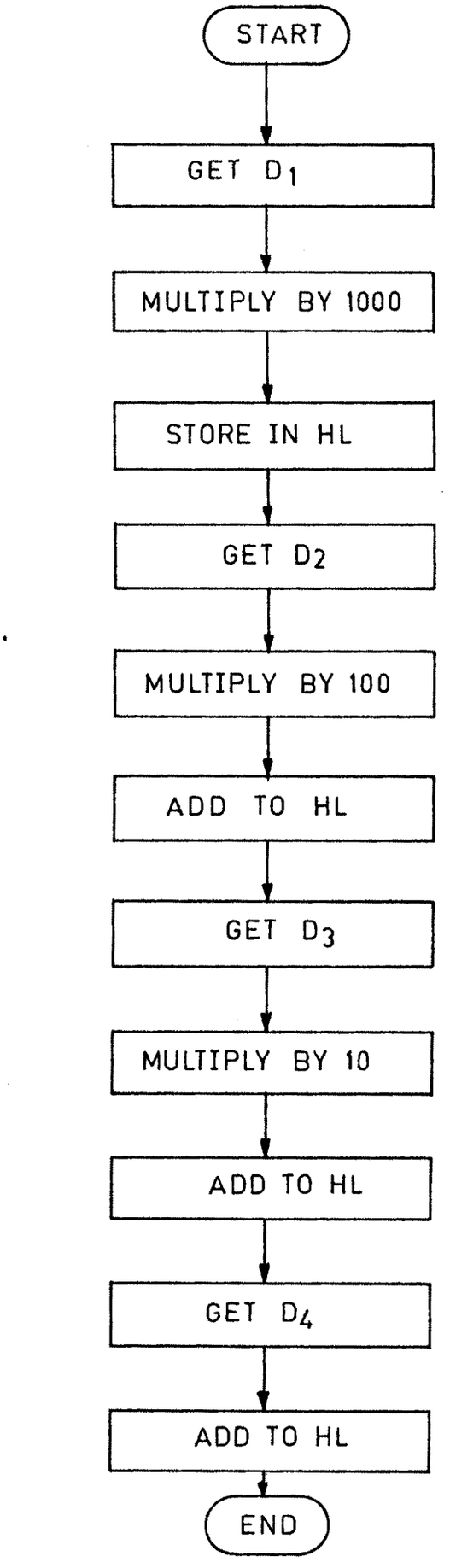


STARTING PROGRAM

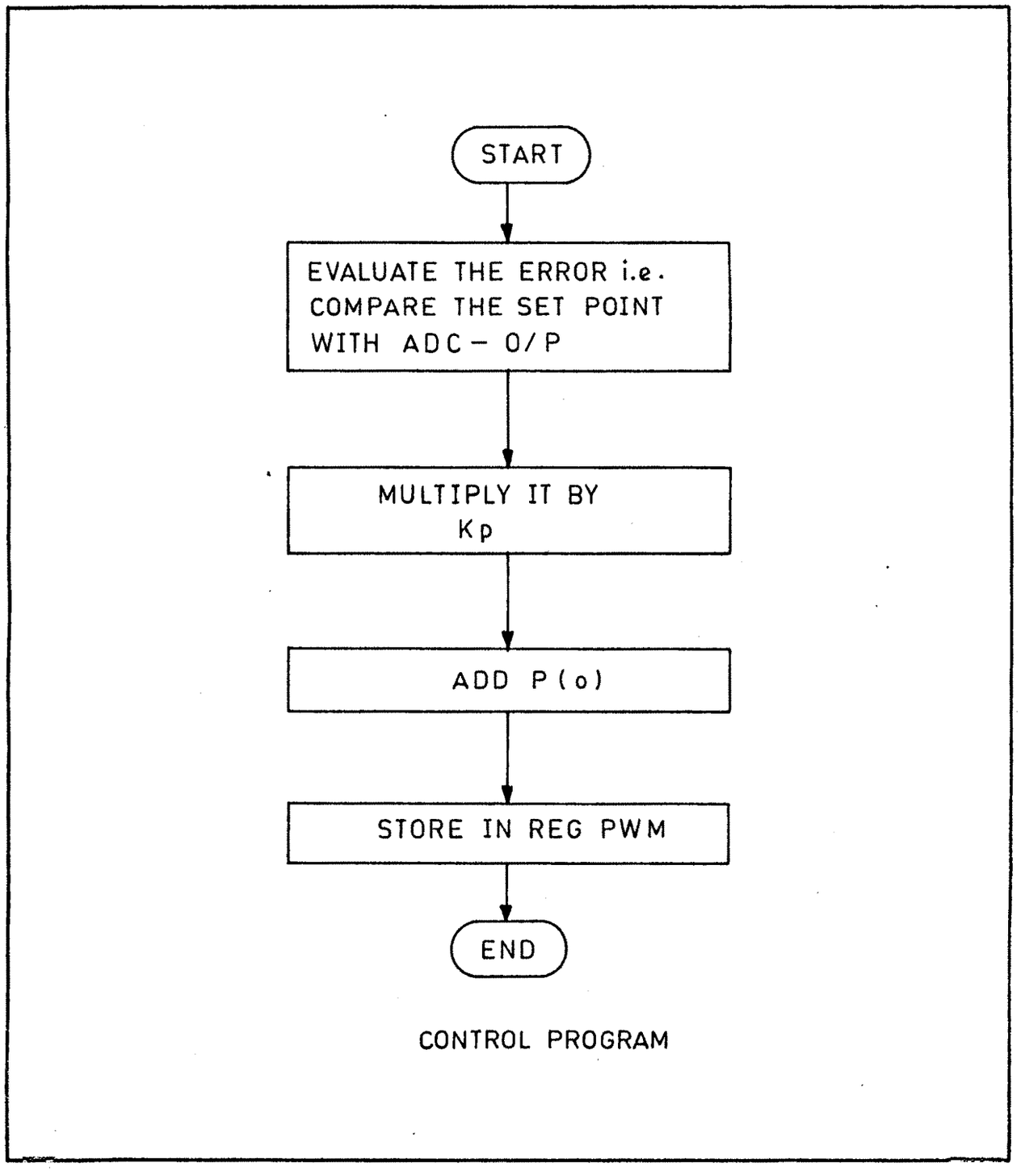

START
IN DATA FROM A-PORT
IS DIGIT STROBE DS1 HIGH
NO
YES
STORE DIGIT(D1) MSB
IN DATA FROM A-PORT
IS DIGIT STROBE DS2 HIGH
NO
YES
STORE DIGIT D2
IN DATA FROM A-PORT
IS DIGIT STROBE DS3 HIGH
NO
YES
STORE DIGIT D3
IN DATA FROM A-PORT
IS DIGIT STROBE DS4 HIGH
NO
YES
STORE D4 LSB
END



PACKED BCD PROGRAM



BCD TO BINARY CONVERSION



CONTROL PROGRAM

4.8 Support chips :(2)

8212 : It is 8-bit I/O port. Its characteristics are.

1. Fully parallel 8-bit data register and Buffer.
2. Service request flip-flop for interrupt generation.
3. Low input load current -0.25 mA Maximum.
4. Three state output.
5. Output sink 15 mA.
6. 3.65 V output high voltage for direct interface to 8008, 8080A, or 8085A CPU.
7. Asynchronous Register clear.
8. Replaces buffers, latches and multiplexers in microcomputer systems.
9. Reduces system package count.
10. Available in express.

- Standared temperature range.
- Extended temperature range.

The pin configuration is given below Fig. 4.7

The 8212 is I/O port consisting of 8-bit latch with 3-state output buffers along with control and device selection logic, also included is a service request flip-flop for the generation and control of interrupts to the microprocessor. The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a micropomputure system can be implemented with that device.

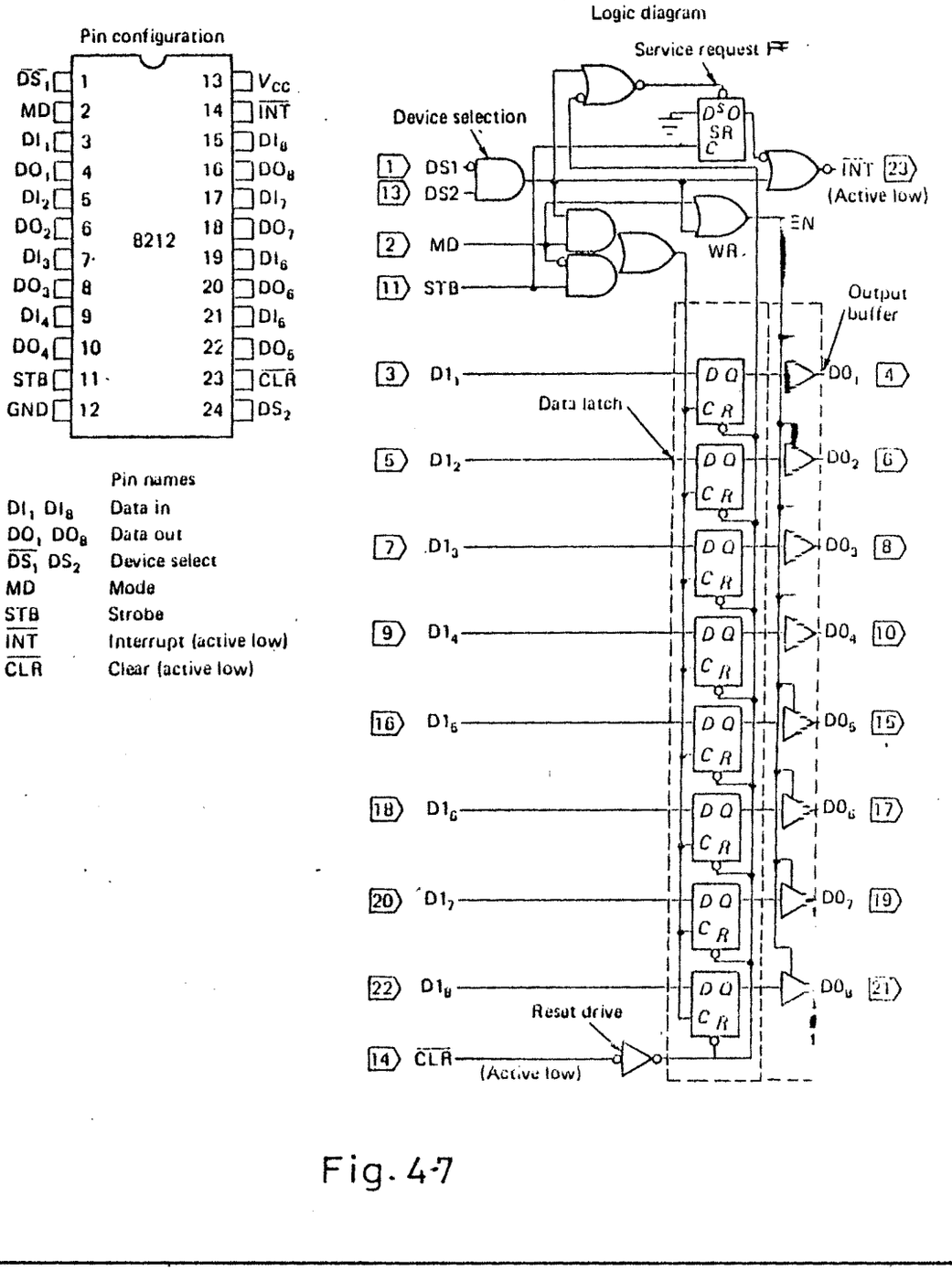

Pin configuration
8212
Pin names
DI1 DI8 Data in
DO1 DO8 Data out
DS1 DS2 Device select
MD Mode
STB Strobe
INT Interrupt (active low)
CLR Clear (active low)
Logic diagram
Service request
Device selection
Output buffer
Data latch
Reset drive
(Active low)

Fig. 4-7

Functional Description :

Data latch : The 8 bflip-flops that make up the data latch are of a "D" type design. The output Q of the flip-flop will follow the data input (D) while the clock output (C) is high. Latching will occur when the clock (C) returns low.

The latched data is cleared by an asynchronous reset input ($C\overline{LR}$). Note clock (C) overrides reset ($C\overline{LR}$).

Output buffer : The outputs of the data latch Q are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); This control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output in to a high impedance state (3-state).

The high impedance state allows the designer to connect the 8212 directly in to the microprocessor bi-directional data bus.

Control logic : The 8212 has control inputs. $\overline{DS}_1$, DS_2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop, $\overline{DS}_1$ $\overline{DS}_2$ (Device select).

These two inputs are used for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1$, $\overline{DS}_2$) the device is selected. In the selected state the output buffer is enable and the service request flip-flop (SR) is asynchronously set.

MD (Mode) : This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic. ($\bar{D}\bar{S}_1$, $\bar{D}S_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\bar{D}\bar{S}_1$. DS_2) and the source of clock (C) to the data latch is the STB (strobe) input.

STB (Strobe) :

This input is used as the clock (C) to the data latch for the input mode (MD=0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request flip-flop :

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip flop is set, It is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device

selection logic ($\bar{D}\bar{S}_1$. DS_2) The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to the active low input priority generating circuits.

4.9 74193 : It is dual 1 of 4 decoder. Its features are.

i) Schottky process for high speed.

ii) Multifunction capability.

iii) TWO completely independent 1 of 4 decoders.

iv) Active low mutually exclusive outputs.

v) Each of the two decoders has 4 output demultiplexer.

The pin diagram is given in fig. 4.8.

Its operating voltage is + 5 volt within the temperature range 0 to $70^{o}C$.

Pin names	Description
A_0, A_1	Address inputs
$\bar{E}$	Enable input (Active low)
$\bar{O}_o$ - $\bar{O}_3$	Outputs (Active low)

4.10 2732 : It is 4K X 8 UV erasable PROM. Its features are

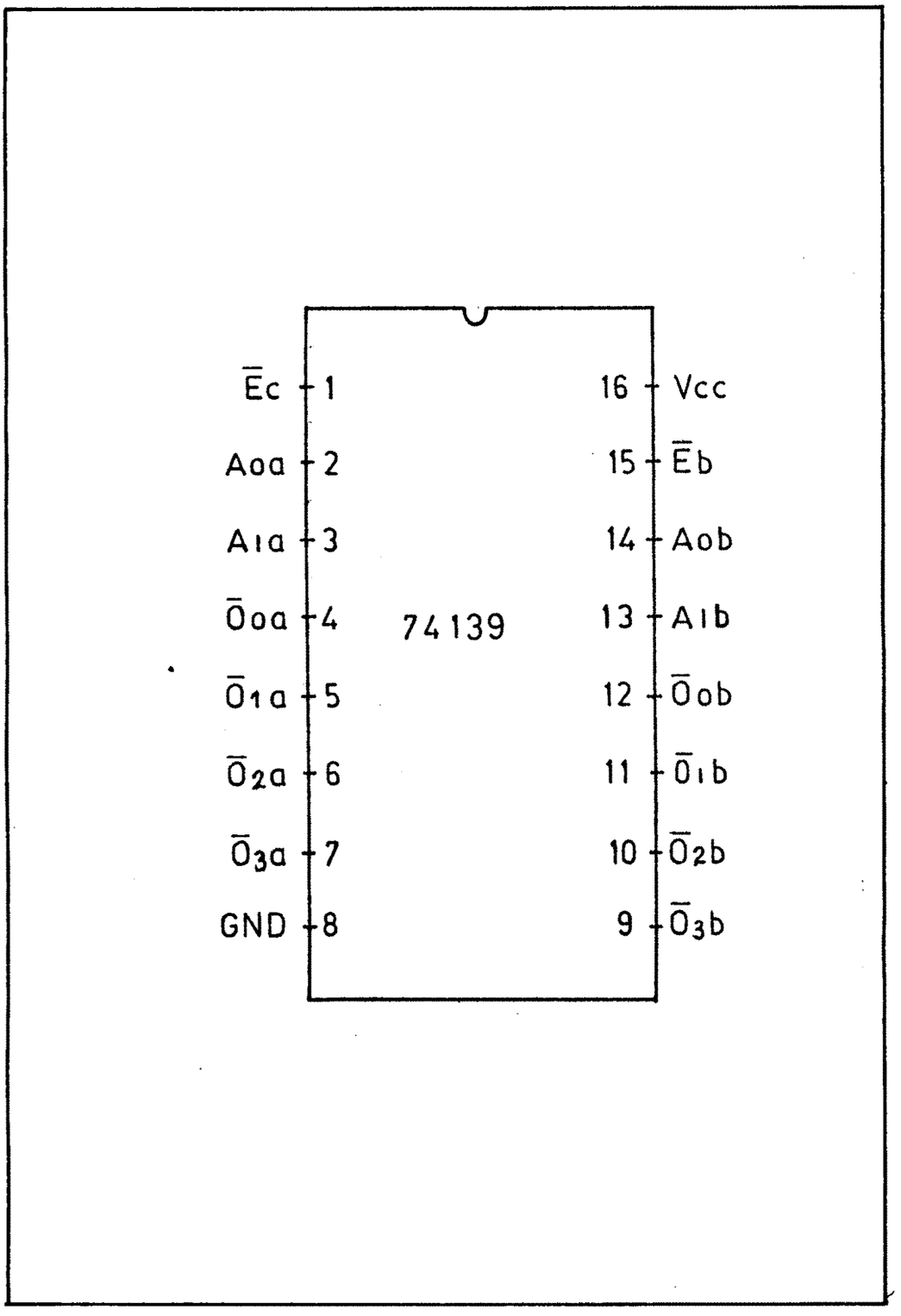
i) Fast access time : - 450 ns Maximum 2732

- 550 ns Maximum 2732-6

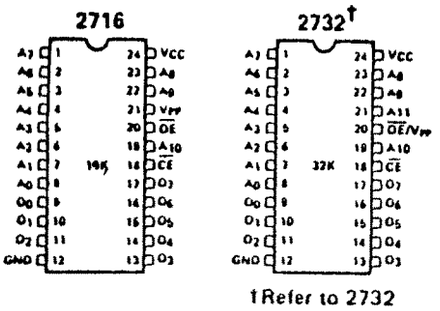
ii) Single + 5 V $\pm$ 5% power supply.

iii) Output Enable for MCS - 85 and MCS 86 Compatibility.

iv) Low power dissipation.


$\overline{E}c$ 1
A0a 2
A1a 3
$\overline{O}$0a 4
$\overline{O}$1a 5
$\overline{O}$2a 6
$\overline{O}$3a 7
GND 8
74139
16 Vcc
15 $\overline{E}$b
14 A0b
13 A1b
12 $\overline{O}$0b
11 $\overline{O}$1b
10 $\overline{O}$2b
9 $\overline{O}$3b

PIN CONFIGURATION*



†Refer to 2732 data sheet for specifications

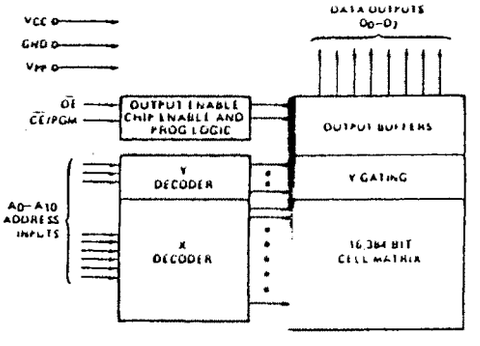
PIN NAMES

A_0–A_8	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



- 150 mA Maximum active current.

  30 mA Maximum standby current.

v) Pin compatible to Intel 2716 EPROM.

vi) Completely static.

vii) Simple programming requirements .

- Single location programming.
- Programs with one 50 ms pulse.

viii) Three-state output for direct bus interface.

The pin out and the mode selection details are given.

Pin names	
$A_o - A_{11}$	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$O_o - O_7$	Outputs

4.11 8155 : (4, 5) : Fig. 4.8 shows the block diagram of Intel 8155 static MOS RAM which has 256 bytes.

It has two programmable 8-bit ports port A and P port B. There are 8-bits in each port which can be programmed, i.e. can be used as input or input by programming the command status register also in the RAM chip.

The memory of I/O port section is addressed using the 8-bit AD bus whether the address on the AD bus is for

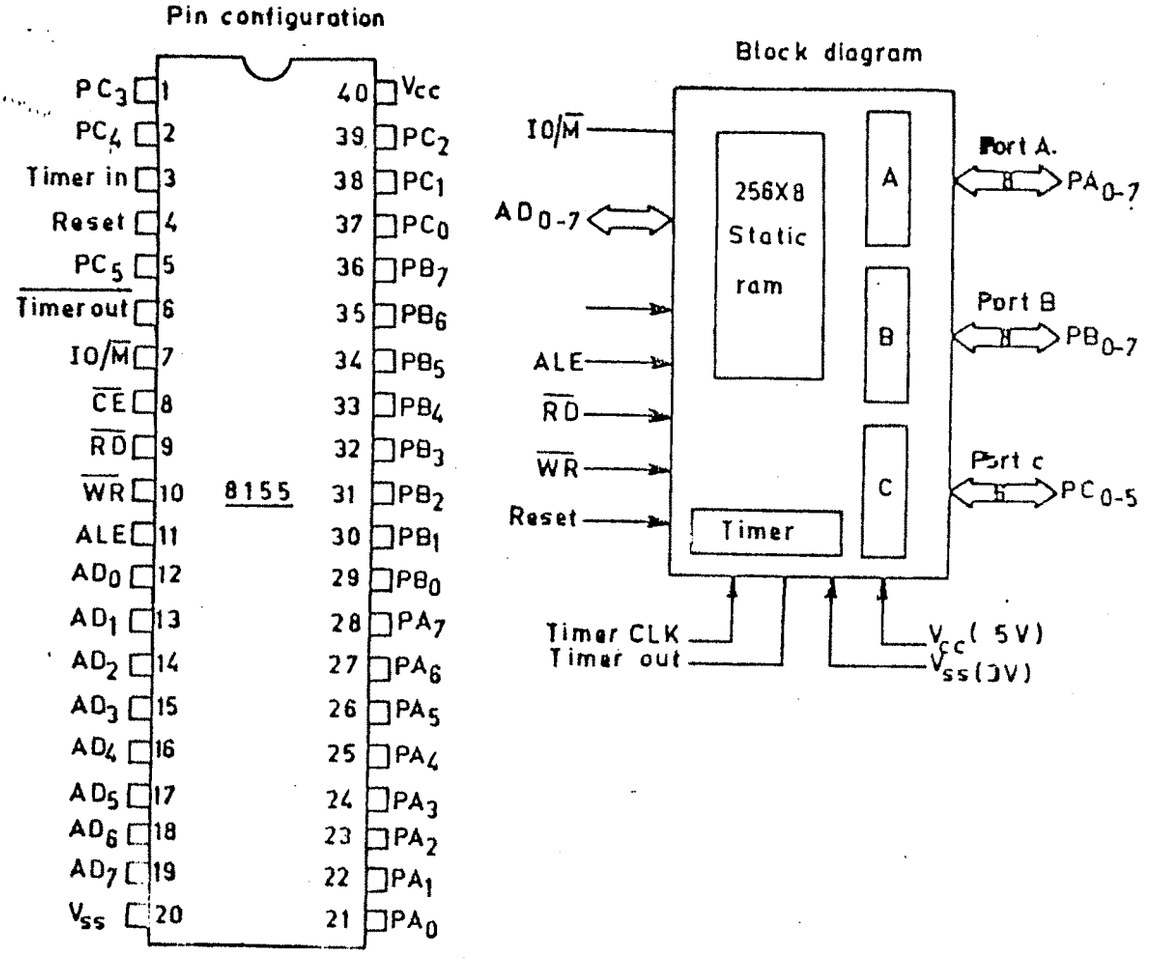


Fig.4-8 Block diagram of 8155

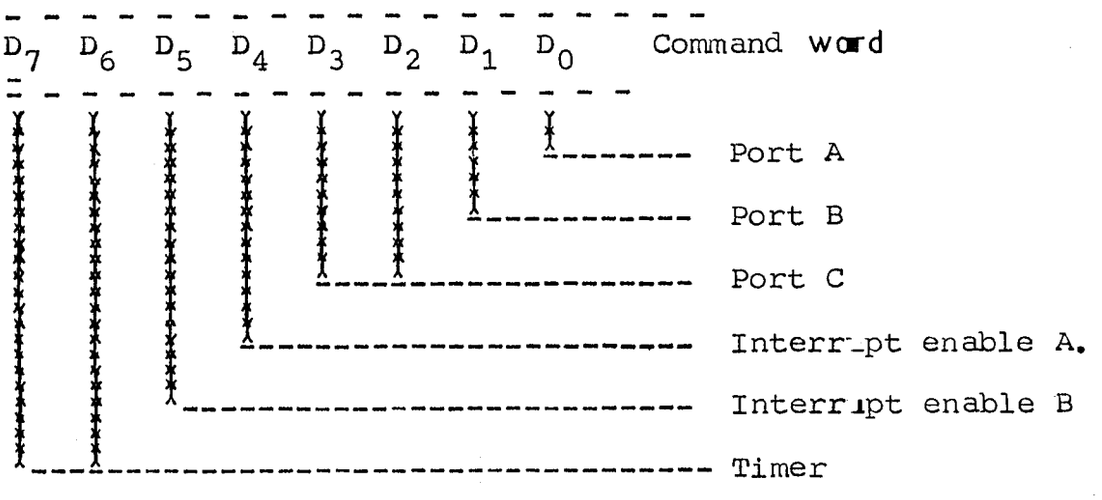
memory or an I/O port depends on the status of the $I_O/\overline{M}$ line. The I/O section is selected if it is 1, and the memory is selected. If it is zero (0). The same AD bus is used for data transfer to and from the microprocessor. To read from memory or any I/O port, $\overline{RD}$ is kept low and $I_O/\overline{M}$ is used as described earlier. Similarly, to write in to the memory or $I/_O$ port $\overline{WR}$ is used and hence again $I_O/\overline{M}$ is used according to the same convention.

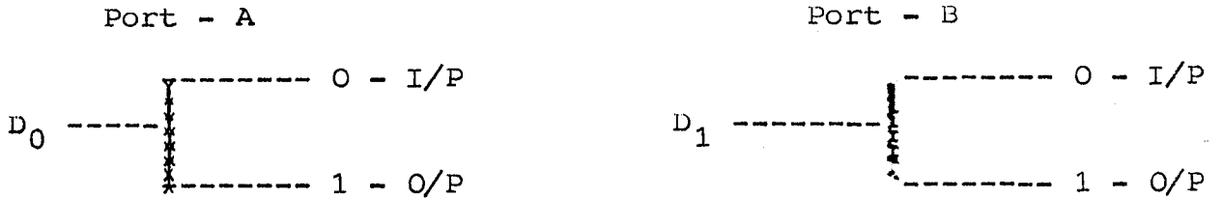
There is a 6-pin port, port C, which can function as input or output port or it provides control signals for ports A and B. Programming of port C is also done through the C/S Register.

The RESET pulse to initialize the system may be provided by the microprocessors on RESET in line. Input high on this line Resets the chip and initializes the three $I/_O$ ports to input mode CE. Input is used for enabling the chip. The 8155 also has a 14-bit programmable binary counter/timer to provide either a sequare wave or terminal count pulse for use in timing of any desired operation. The $I/_O$ addresses are given in Table 4.

Table - 4

AD_2	AD_1	AD_0	Location
0	0	0	Command and status register.
0	0	1	Port A
0	1	0	Port B
0	1	1	Port C
1	0	0	Low 8-bit of timer
1	0	1	2 bits of time mode and upper 6-bits of timer.

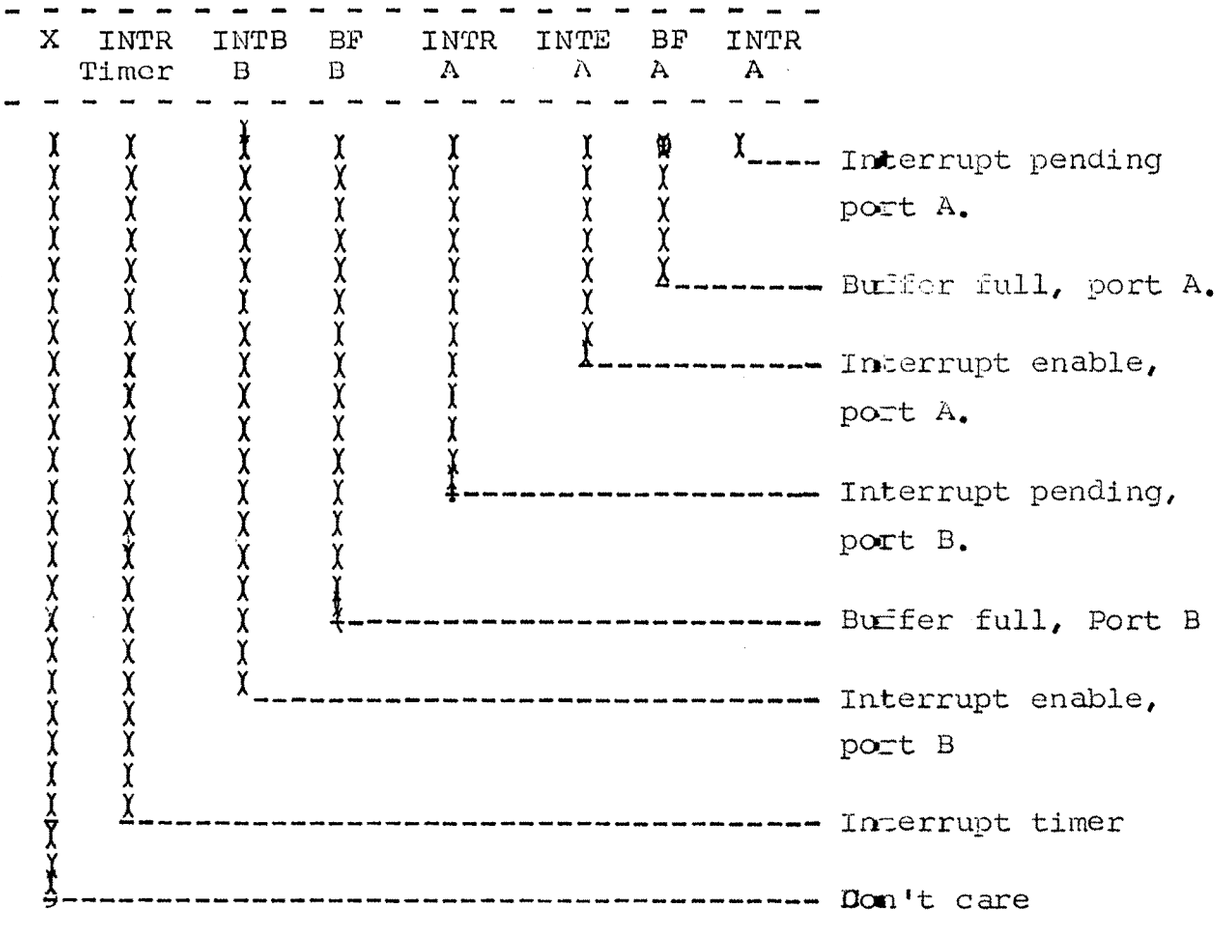




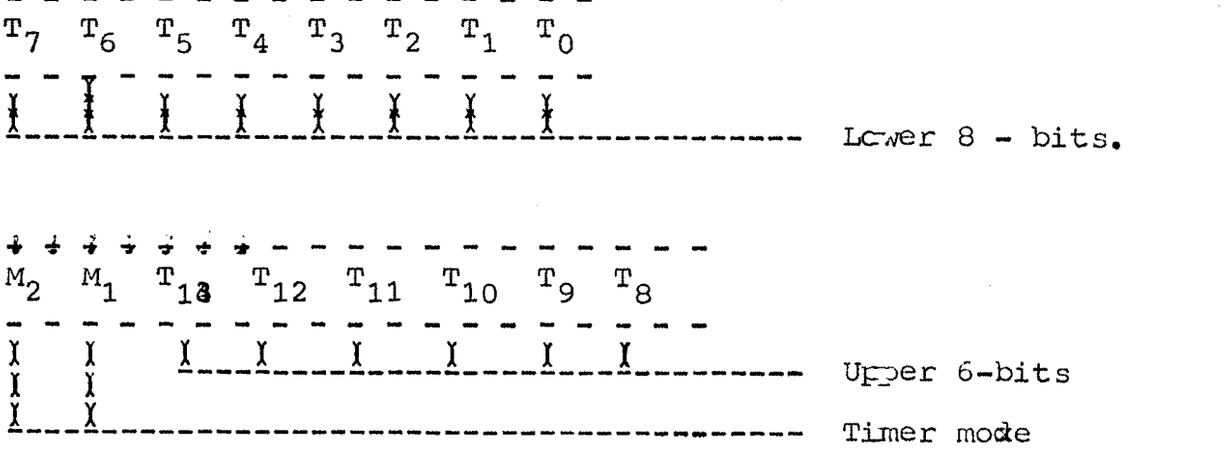
Port C

D_3	D_2	Mode
0	0	I/P port 9 (6-bits)
0	1	Port A handshaking and (3-bits
1	0	Ports A and B handshaking
1	1	O/P port C(6-bits)

Status word



Timer program : The lower and the upper time bytes are shown.



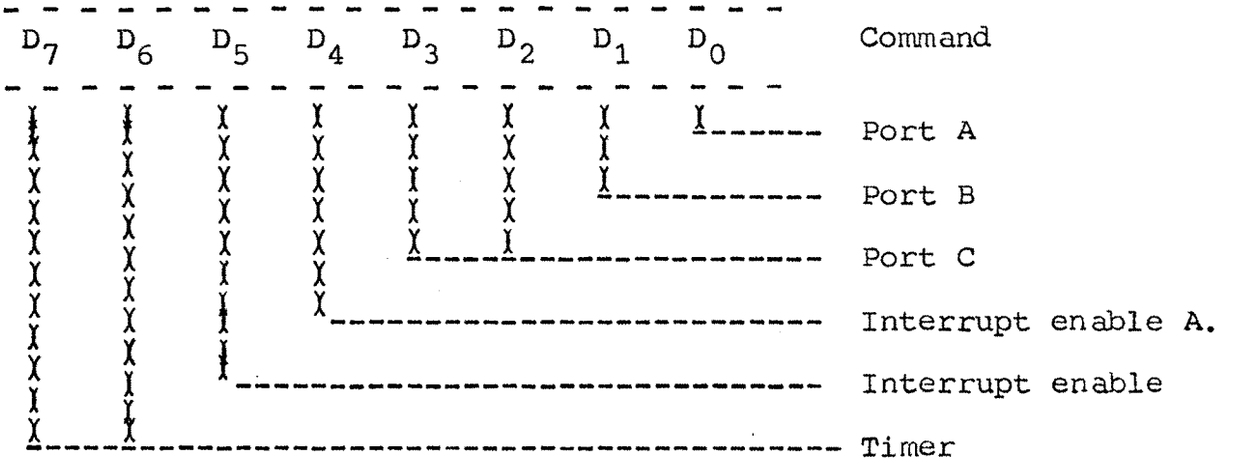
Timer mode

M_2	M_1	Effect
0	0	Single square wave
0	1	Continuous square wave
1	0	Single pulse
1	1	Continuous pulse

Timer Command

D_7	D_6	Effect
0	0	Nop
0	1	Stop immediately
1	0	Stop after TC is reached
1	1	Start

Timer commands bits



MOTOROLA

MC14433

3½ DIGIT A/D CONVERTER

The MC14433 is a high performance, low power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range from 1.999 volts to 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

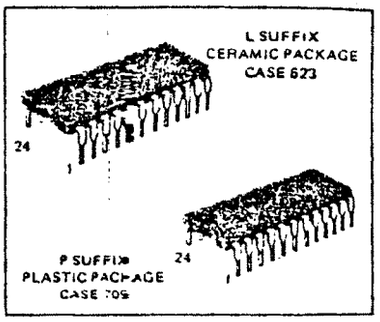
The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions/s
- Z_{in} > 1000 M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs—Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Low Power Consumption: 8.0 mW typical @ ±5.0 V
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

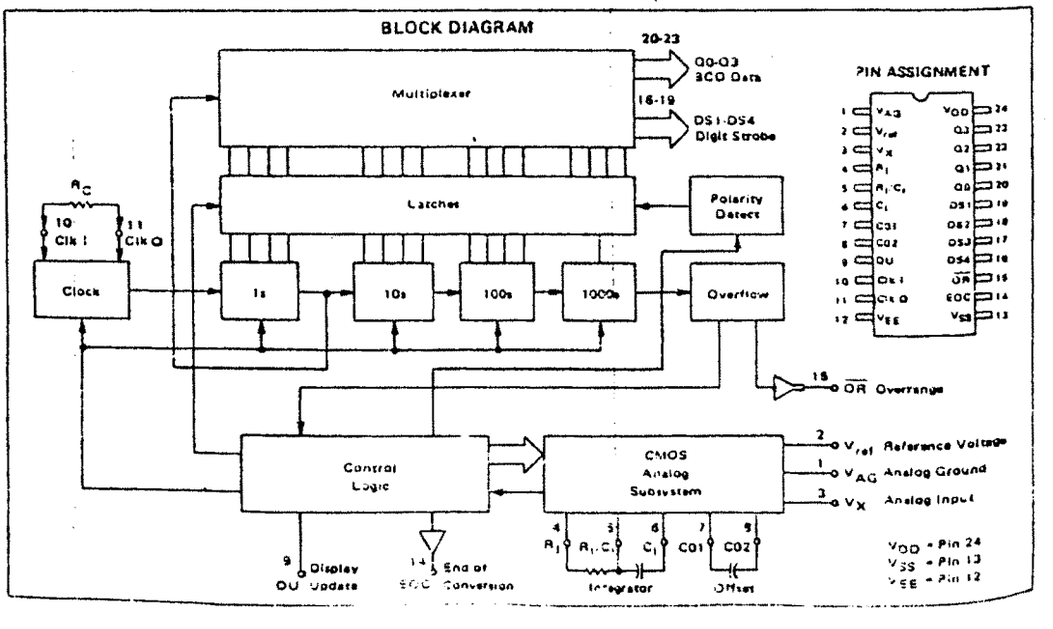
3½ DIGIT A/D CONVERTER



ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to -18	Vdc
Voltage, any pin, referenced to V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_o	0.1 ± 20%	µF

ELECTRICAL CHARACTERISTICS (C_I = 0.1 µF mylar, R_I = 470 kΩ @ V_{ref} = 2.000 V, R_I = 27 kΩ @ V_{ref} = 200.0 mV, C_o = 0.1 µF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Linearity-Output Reading (Note 1)	–										%rdg
(V_{ref} = 2.000 V)		5.0	-5.0	–	–	-0.05 -Count	±0.05	+0.05 +Count	–	–	
(V_{ref} = 200.0 mV)		5.0	-5.0	–	–	–	±0.05	–	–	–	
Stability-Output Reading (Note 2)	–										LSD
(V_X = 1.990 V, V_{ref} = 2.000 V)		5.0	-5.0	–	–	–	–	2	–	–	
(V_X = 199.0 mV, V_{ref} = 200.0 mV)		5.0	-5.0	–	–	–	–	3	–	–	
Zero-Output Reading (V_X = 0 V, V_{ref} = 2.000 V)	–	5.0	-5.0	–	–	–	0	0	–	–	LSD
Bias Current — Analog Input	–	5.0	-5.0	–	–	–	±20	±100	–	–	pAdc
Reference Input		5.0	-5.0	–	–	–	±20	±100	–	–	
Analog Ground		5.0	-5.0	–	–	–	±20	±500	–	–	
Common Mode Rejection (V_X = 1.4 V, V_{ref} = 2.000 V, f_{oc} = 32 kHz)	–	5.0	-5.0	–	–	–	65	–	–	–	dB
Output Voltage — Pins 14 to 23											Vdc
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	-5.0	4.95	–	4.95	5.0	–	4.95	–	
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	–	4.95	–	-5.0	-4.95	–	-4.95	
"1" Level	V_{OH}	5.0	-5.0	4.95	–	4.95	5.0	–	4.95	–	
Output Current — Pins 14 to 23											mAdc
(V_{SS} = 0 V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	–	-0.2	-0.38	–	-0.14	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.82	–	-0.5	-0.9	–	-0.35	–	
(V_{OL} = -4.5 V) Sink	I_{OL}	5.0	-5.0	1.6	–	1.3	2.25	–	0.9	–	
Clock Frequency (R_C = 300 kΩ)	f_{Clk}	5.0	-5.0	–	–	–	66	–	–	–	kHz
Input Current — DU	I_{DU}	5.0	-5.0	–	±0.3	–	·000001	±0.3	–	·1.0	µAdc
Quiescent Current	I_Q	5.0	-5.0	–	3.7	–	0.9	2.0	–	.6	mAdc
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	-8.0	–	7.4	–	1.8	4.0	–	3.2	
DC Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2.000V)	–	5.0	-5.0	–	–	–	0.5	–	–	–	mV/V

Note 1: Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

Note 2: 3 LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.

digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An interdigit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus, with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select ouptut and EOC signals is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the ½ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin.

TRUTH TABL

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding	
+0	1	1	1	0	Blank	
−0	1	0	1	0	Blank	
+0 UR	1	1	1	1	Blank	
−0 UR	1	0	1	1	Blank	
+1	0	1	0	0	4 → 1	Hook up
−1	0	0	0	0	0 → 1	only seg b
+1 OR	0	1	1	1	7 → 1	and c to
−1 OR	0	0	1	1	3 → 1	MSD

Notes for Truth Table
Q3 — ½ digit, low for "1", high for "0"
Q2 — Polarity: "1" = positive, "0" = negative
Q0 — Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 – ALTERNATE OSCILLATOR CIRCUITS

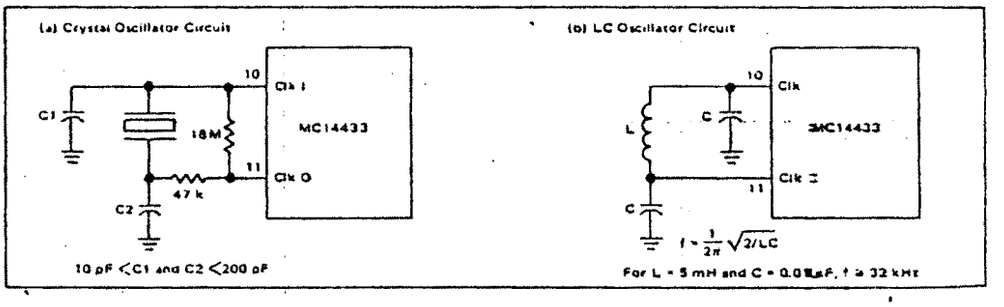


FIGURE 8 – DIGIT SELECT TIMING DIAGRAM

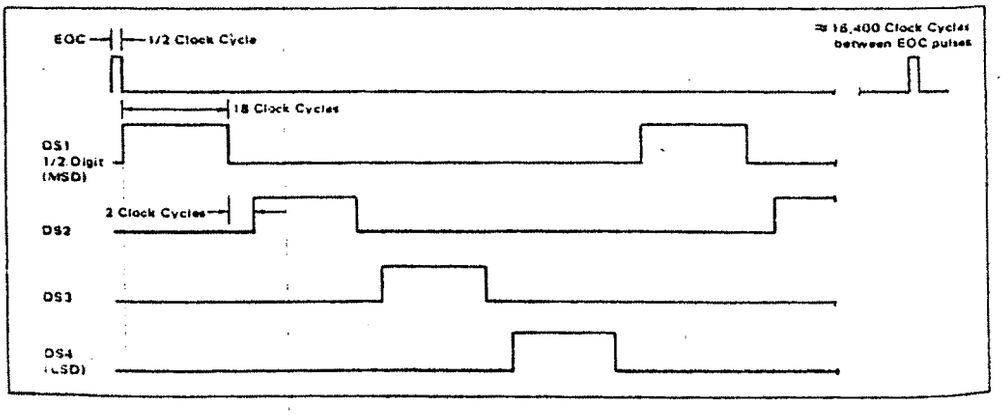


FIGURE 9 – INTEGRATOR WAVEFORMS AT PIN 6

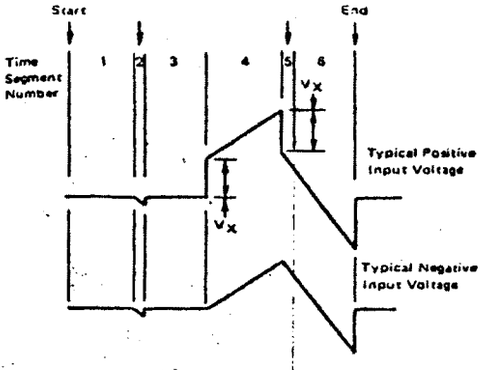
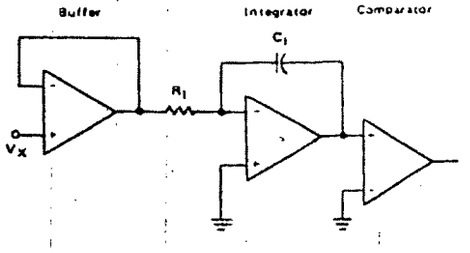


FIGURE 10 – EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offsat voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 – The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 – The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

Segment 3 – This segment of the conversion cycle is the same as Segment 1.

Segment 4 – Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 – This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 – This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR versus POWER SUPPLY SKEW

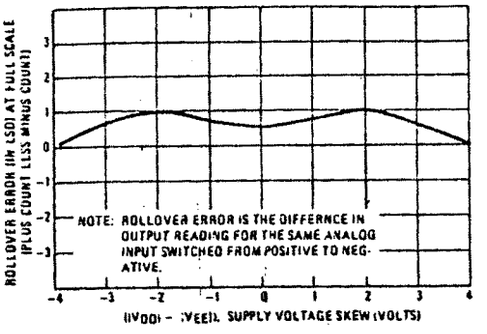


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT versus TEMPERATURE

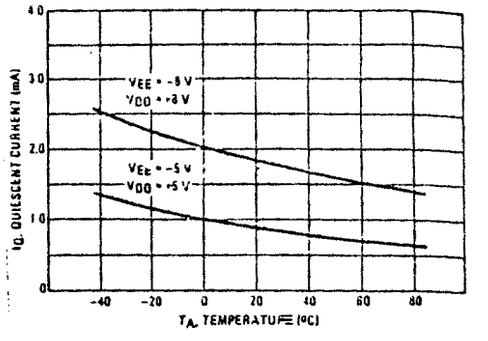


FIGURE 3 – TYPICAL N-CHANNEL SINK CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

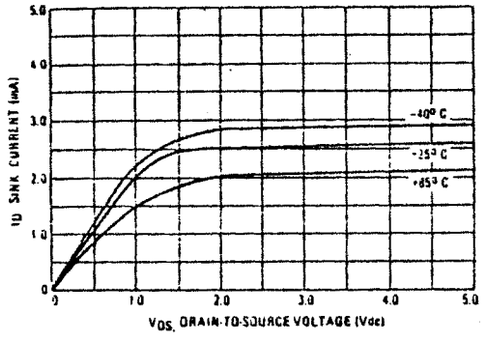


FIGURE 4 – TYPICAL P-CHANNEL SOURCE CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

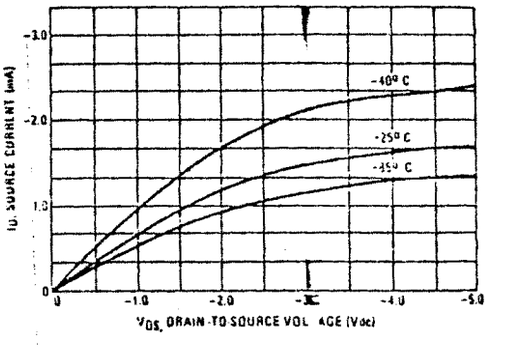


FIGURE 5 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

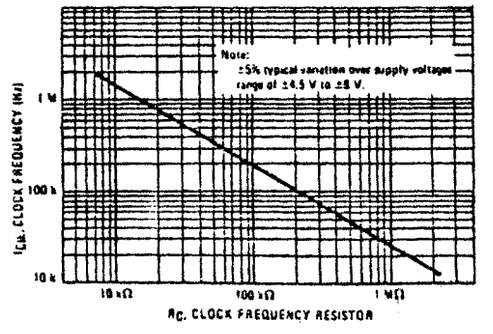
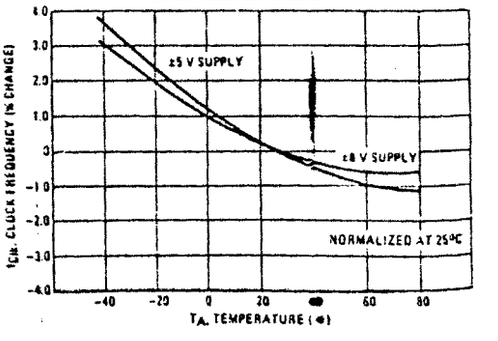


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY versus TEMPERATURE



CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16,400} \pm 1.5\%$
MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$

DEVICE OPERATION

ANALOG GROUND (V_{AG}, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input.

REFERENCE VOLTAGE (V_{ref}, Pin 2)
UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, pin 2 functions as a reset for the A/D converter. When pin 2 is switched to V_{EE} for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I, R_I/C_I, C_I; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μF (mylar) while the resistor should be 470 kΩ for 2.0 V full scale operation and 27 kΩ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(max)}{C_I} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X(max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:

R_I is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{Clk} is the clock frequency at pin 10 in kHz

Example:

$C_I = 0.1$ μF
$V_{DD} = 5.0$ volts
$f_{Clk} = 66$ kHz
For $V_X(max) = 2.0$ volts
$R_I = 480$ kΩ (use 470 kΩ ± 5%)
For $V_X(max) = 200$ mV
$R_I = 28$ kΩ (use 27 kΩ ± 5%)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow $V + V_X$ to exceed V_{DD}. The 0.3 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR (CO1, CO2, Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.

CLOCK (Clk I, Clk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE}. A 300 kΩ resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (V_{EE}, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through pin 13.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY (V_{SS}, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, $\overline{OR}$). When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD}. When connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The allowable operating range for V_{SS} is between $V_{DD} - 7.0$ volts and V_{EE}.

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (pin 11).

OVERRANGE ($\overline{OR}$, Pin 15)

The $\overline{OR}$ pin is low when V_X exceeds V_{ref}. Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1, Pins 16, 17, 18, 19)

The digit select output is high when the respective

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