CHAPTER 3

P C AND IT'S INTERFACING WITH IONOSONDE

3.0 INTRODUCTION:

The ionosonde system has been described in the earlier chapter. The personal computer has been used with appropriate interfacing hardware to fulfill the need of control and digitization of detector output signal, it's A/D, D/A conversion is in the form of daughter board in the computer.

Basically there are two modes of triggering the transmitter; (1) Internal (2) External. In internal mode triggering is synchronized to AC mains and the PRF is either the frequency of mains or half of it. PRF is switch selectable. Therefore for 50 Hz mains PRF is 50/25 Hz. In external triggering mode the trigger pulse is generated through PC for each frame acquisition. Frame is defined as the period (1/PRF) over which data are collected.

The conventional photographic method of recording of the ionogram is replaced by this digital system, that includes ionosonde, personal computer , PC ad on card and amplifier/attenuator. The block diagram of this system or digisonde is shown in chapter second. The ionosonde is explained in detail in previous chapter.

In the absence of appropriate antenna system for BAND I ,II and III a microprocessor based subsystem is used in the place of ionosonde for the simulation of the panaromic display i.e. ionogram. The microprocessor subsystem is used to show only the

simulation. Since a folded dipole antenna system is available for BAND IV for actual ionospheric echo has been used for digitization.

3.1 HARDWARE: Personal Computer :

For processing and storing the data a PC AT/286 computer is used. The system configuration is given below is running under MS DOS 5.0 operating system. For conversion of Analog signal to digital the PC-Add on card is used. The PC→Add on card using AD-574 and DAC(AD-7541AKN) supports the 8 channels for ADC and 1 channel for DAC. The interface connector of 20 pin is on the card, provides the facility of giving 8 channels as an input and single channel as analog output, i.e. equivalent of 12 bit of binary data. The basic configuration is given in article 3.1.1

3.1.1: The PC-AT IBM Compatible Hardware Configuration:

Main processor	: 80286
Clock speed	: 25 MHz.
Floppy drive A	: 1.2 Mb, 5 1/4"
Display type	: Monochrome
Base memory size	: 640 kB
Ext memory size	: 384 kB
Hard disk C	: 40 Mb
Parallel port	: 3BC
Printer	: Epson LX-800

The configuration logic (mode switch input logic) senses the ON/OFF condition of the mode switches (DIP switch). This information is stored in memory by the firmware for future use.

I/O PORT ADDRESSES :

The port addresses in PC are 16 bits in I/O mapped I/O scheme. Hence the CPU addresses the 16 bit I/O ports through INPUT(IN) or OUTPUT(OUT) instruction.

The I/O addresses Hex 000 to 0FFH are reserved for the motherboard. The addresses Hex 100 to 3FFH are available for us in daughter boards Table 3.1 provides an I/O address map for PC.

TABLE 3.1 : I/O ADDRESS MAP

HEX RANGE	USAGE
000-00f	DMA chip 8253A-5
020-021	Interrupt 8259-A
040-043	Timer 8253-5
060-063	PPI 8255A-5
080-083	DMA page register
0AX	NMI
0CX	Reserved
0EX	Reserved
200- 20F	Game control
210-217	Expansion unit
220-24F	Reserved
278-27F	Reserved
2F0-2F7	Reserved
2F8-2FF	Asynchronous communication
300-31f	Prototype card
320-32F	Fixed disk
378-37F	Parallel printer

380-38F	SDLC Communication
3A0-3AF	Reserved
3B0-3BF	IBM monochrome DIsplay
3C0- 3CF	Reserved
3D0-3DF	Color/Graphics
3E0-3E7	Reserved
3f0-3F7	Disket
3F8-3FF	Asynchronous Communications.

I/O CHANNEL :

The arrangement interface connectors(slots) along the back of the system board called I/O channel. These slots are numbered J1 through J8. Using these peripheral slots one can interface the computer to outside world devices.

I/O channel is an extension of system bus. The I/O channel contains an 8 bit bidirectional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read and write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines and power and ground for the adapters four voltage lines are provided for I/O channels : +5V dc. -5V dc, +12V dc and -12V dc. These functions are provided in a 62-pin connector with 100 mil card tab spacing for IBM compatible machines.

I/O CHANNEL DESCRIPTION :

I/O channel diagram is shown in fig 3.1. The following is description of the IBM PC I/O channel. All lines are TTL compatible.

In the above connector external PC Add on card can be

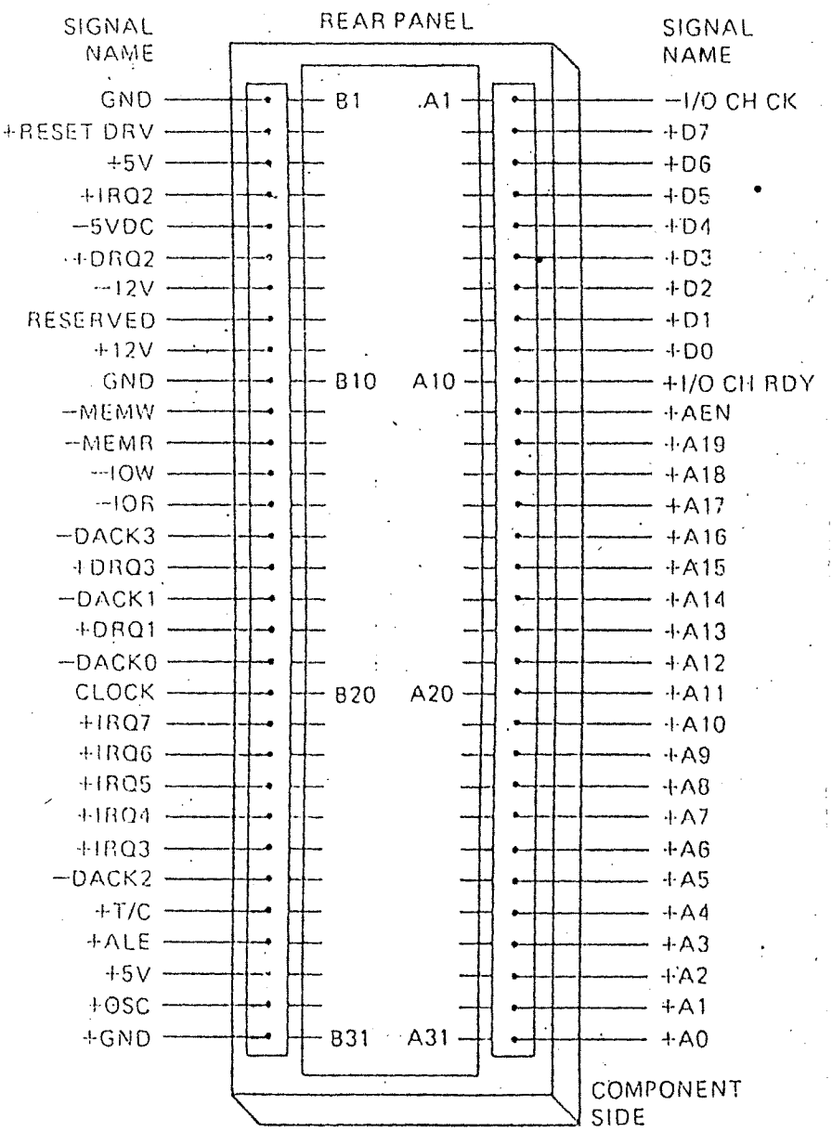


FIGURE 13-1 Pin names and numbers for peripheral slots on IBM PC motherboard.

placed in such way that all above signals are linked on the card used for conversion of data. In next article the detailed description is given of 12 bit AD-DA card which is used for number of devices along with computer for data acquisition purpose.

3.2 12 BIT HIGH PERFORMANCE A/D -D/A CARD :

The block diagram of AD/DA card is shown in fig 3.2. The base address is selectable by the DIP switch. When the software routine addresses the DIP switch address, the card is enabled. The reference voltage generator produces the desired reference voltage which are jumper selectable .

In the D/A operation, any 12 bit binary number which is input from the PC-bus is fed to the latch through the data buffer. The latched digital values is fed to the DAC logic for D/A conversion. The analog output is fed to a buffer and finally to the 20 pin FRC connector.

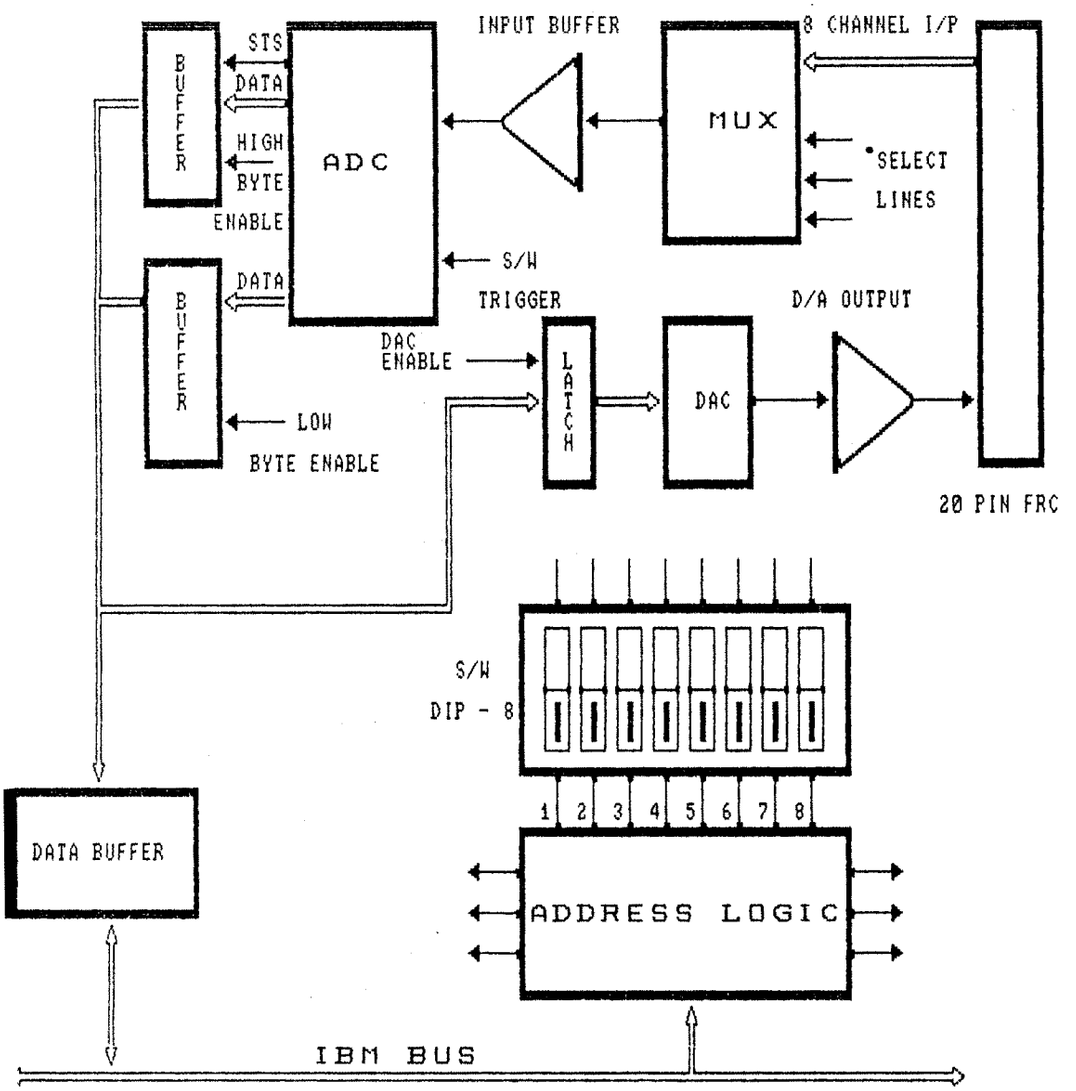
In the A/D operation, any one of the 8 channels present on the 20 pin FRC can be selected by the MUX. For impedance matching the input signal is buffered and then fed to the ADC. The ADC can be software triggered by outputting the required data through the specific address register. The converted data can be read through two latches, one containing the higher byte and the other, lower byte. The data is fed to the IBM-PC bus through the data buffer.

The specifications of the PC add on card are as fallows.

1) Eight single -ended analog input channels.

2) An industrial standard 12-bit successive approximation converter (ADC-574) used to convert analog inputs voltages.

3) The maximum conversion time is 25 microseconds.



IG.3.2 BLOCK DIAGRAM OF A PC ADD-ON CARD

4) Analog input range : -5 to +5 volt

5) Accuracy : 0.015 % of reading +/-1 bit.

6) Linearity : +/-1 bit.

7) The A/D trigger and data transfer is controlled by the software.

8) Power consumption

+5v : typ. 100 mA, max. 500 mA.

+12v : typ. 40 mA, max. 100 mA.

-20v : typ. 20 mA, max. 50 mA.

9) I/O connector

20 pin post header for analog I/O ports.

10) I/O base address

Requires 16 consecutive address locations. Base address defined by the DIP switch for address lines A9-A4.

(current setting is Hex 220)

For current settings of the address and the functions are assigned as in table 3.2.1.

TABLE 3.2.1: **ADDRESS DEFINED FOR FUNCTIONS:**

LOCATION	READ	WRITE
BASE + 0	N/U	N/U
BASE + 1	N/U	N/U
BASE + 2	N/U	N/U
BASE + 3	N/U	N/U
BASE + 4	Read ADC lower byte	D/A low byte
BASE + 5	Read ADC upper byte	D/A high byte
BASE + 6	N/U	N/U
BASE + 7	N/U	N/U

BASE + 8	N/U	N/U
BASE + 9	N/U	N/U
BASE + 10	N/U	MUX scan channel
BASE + 11	N/U	Software A/D trigger
BASE + 12	N/U	Software A/D trigger
BASE + 13	N/U	N/U
BASE + 14	N/U	N/U
BASE + 15	N/U	N/U

NOTE : N/U = Not used

The channel is selected using software by setting D0 to D2 bits at data lines. The address of channel is latched using D-latch. The multiplexer switches to a new channel when channel address to this is changed. Data format for eight analog channels is given in table 3.2.2. below.

TABLE 3.2.2: **DATA FORMAT:**

BASE +10 SCAN CHANNEL	D7	D6	D5	D4	D3	D3	D2 A2	D1 A1	D0 A1
Channel 0	X	X	X	X	X	X	0	0	0
Channel 1	X	X	X	X	X	X	0	0	1
Channel 2	X	X	X	X	X	X	0	1	0
Channel 3	X	X	X	X	X	X	0	1	1
Channel 4	X	X	X	X	X	X	1	0	0
Channel 5	X	X	X	X	X	X	1	0	1
Channel 6	X	X	X	X	X	X	1	1	0
Channel 7	X	X	X	X	X	X	1	1	1

NOTE X = don't care lines

A0, A1, A2 = Scan channel address.

20 pin FRC connector accessible through the rear of the PC. The pin assignment of this connector is given in Table.3.2.3.

TABLE 3.2.3: **TABLE OF CONNECTOR PIN ASSIGNMENT:**

SIGNAL NAME	PIN NO.	PIN NO.	SIGNAL
A/D 0	1	2	A. GND
A/D 1	3	4	A. GND
A/D 2	5	6	A. GND
A/D 3	7	8	A. GND
A/D 4	19	10	A. GND
A/D 5	11	12	A. GND
A/D 6	13	14	A. GND
A/D 7	15	16	A. GND
D/A	17	18	A. GND
A. GND	19	20	A. GND

NOTE : A/D - Analog input

A. GND - Analog ground

D/A - Analog output

Initially the channel is defined by writing it's address in case of A/D operation, start conversion pulse is addressed to either BASE+11 or BASE+12 depending on switch SW7 and SW8. Check the status of EOC. The high to low transition is nothing but conversion is over. read upper byte first, mask bit D4 and then

read lower byte . As per data format given below.

UPPER BYTE								LOWER BYTE							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

where first three bit's from left are not to be considered, fifth (D4) bit EOC status bit, remaining 12 bit's are valid bits; which represents the data.

For D/A operation write first lower byte to base address BASE+4 and higher byte to BASE+5. It's equivalent analog is on pin no. 17 of FRC connector.

The software is developed under HLL and ALP languages and are interfaced, which is explained in chapter 4.

3.3 MICROPROCESSOR BASED SIGNAL SIMULATION : (SUBSYSTEM)

For simulation, the identical signals to the ionosonde are derived with the use of single board computer. Single board computer based on 8085A CPU is designed specially for training and development applications. The response of present transmitting and receiver folded dipole antenna is good in only fourth band i.e 6.75 to 20.25 MHz. Remaining three bands suffer attenuation by mismatch of antenna impedance. Therefore single board computer is equally useful for our system simulation. Using single board computer the `A' scope signals are developed with various delays corresponding to the ground and echo pulses.
The system specifications are as follows:-

SUBSYSTEM HARDWARE OVERVIEW :

Central processing unit : Single board computer is based on the INTEL 8085A. high performance CPU operating at 3

MHz.

Memory : Powerful system monitor has been provided on 2732 EPROM covering 4K bytes. This monitor includes all standard commands codes, functions and utility subroutines. A 6116 battery back up RAM (2K) is provided on board for inputing and executing programs.

Hex keypad/display interface : A keypad with 21 keys and 6 digits LED seven segment display is provided for interaction with the system using 8279 keyboard/display controller. This chip provides the following feature.

Simultaneous keyboard and Display operation scanned keyboard Model sensor mode 2 key lockout/N key roll over. contact Debounce 16 Displays.

Programmable scan timing.

The hex keypad has the standard hexadecimal keys and many other function and code keys. 4 User Definable function keys are also provided which can be defined by the user. All scan, return, shift and control lines of 8279 are brought on to connector J4.

8279 Data format : The data format for the character being displayed by the 8279 is one bit corresponding to each segment of the seven segment display plus one bit for the decimal point. The display bits are store in the 8279 in the form of one byte per digit of the display from RAM location 0 to 5. The format is as follows:

A3	A2	A1	A0	B3	B2	B1	B0
c	d	b	a	e	g	f	dp

Parallel I/O interface : 46 parallel I/O lines are provided on board, 22 from 8155 and 24 from 8255. These lines are brought on to connector J2 and J3, for 8155 respectively.

Serial I/O + Audio cassette Interface : Serial I/O is available through RS232C compatible port. The SID and SOD lines are used under software control for serial operation. Baud rate is auto adjustable. Onboard audio cassette I/F is provided with file management, for storage and retrieval of data using a cassette recorder.

Timer : Three channel of 8255 chip, a 16 bit Timer counter and one channel of 14 bit Timer/Counter of 8255 are provided on board. All lines of 8255 are provided on connector J7 and lines of 8155 are provided on J2.

FIRMWARE OVERVIEW:

The system has very powerful and user friendly FIRMWARE in the 2732 EPROM. One can borrow any subroutine from the listing for his own program development. Various commands available through the keyboard and the coded subroutines are accessible through the CODE key. An important point here about the FIRMWARE is the option of entry point to the monitor. There are two options available, one is the COLD START, other is WARM START. In cold start entry the system is completely reinitialized and no user program status is saved from the previous program executed. This is equivalent to the hardware reset. COLD START entry can be performed through software by using the RST 0 instruction. In WARM start entry the start of previously executed user program is fully saved before entering the monitor. WARM START entry is possible through software by using the RST 1 instruction.

CONNECTOR AND STRAPPING DETAILS :

The single board computer has seven connector on board and are listed below.

J1 : 50 pin edge connector with STD compatible

J2 : 26 pin flat cable connector for 8155

J3 : 26 pin flat cable connector for 8255

J4 : 26 pin flat cable connector for 8279

J5 : 7 pin power supply

J6 : 7 pin for serial I/O

J7 : 10 pin FRC connector for 8253.

From above list the useful connector pin configuration i. e. J3 is given below in table 3.3.1.

TABLE 3.3.1: **CONNECTOR J3:**

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	PA3	2	PA2
3	PA1	4	PA0
5	VCC	6	PA7
7	PA6	8	PA5
9	PA4	10	PC7
11	PC6	12	PC5
13	PC4	14	PC0
15	PC1	16	PC2
17	PC3	18	PB0
19	PB1	20	PB2
21	PB3	22	PB4

23	PB5	24	PB6
25	PB7	26	GND

The system supports Add-On cards interface, such as D/A ,A/D steeper motor etc. The present system is interfaced with D/A card, Through PPI connector J3 (8255).

The digital to analog converter card circuit diagram is shown in fig. 3.3.

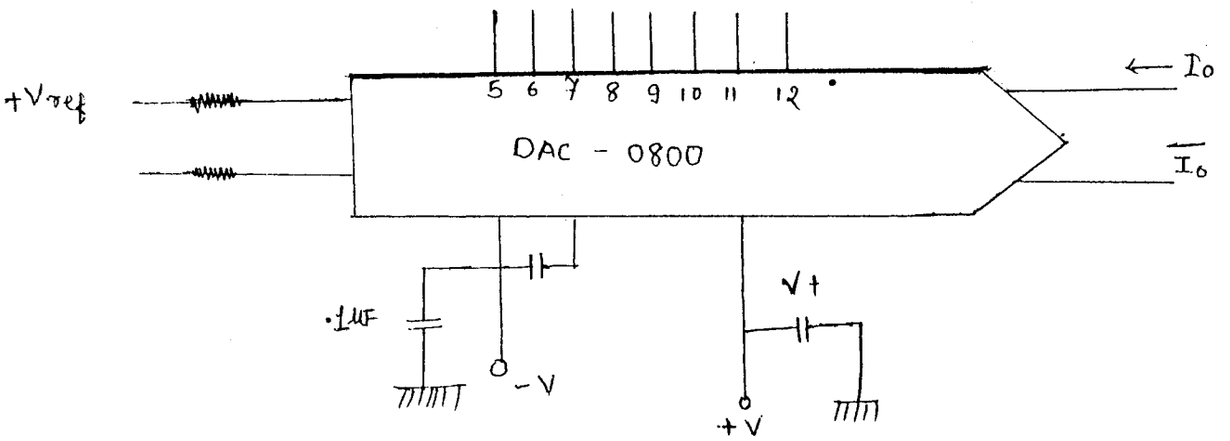


FIG 3.3: Digital to analog converter.

Digital to analog converter interface card is designed around DAC 0800 monolithic 8 bit high speed current output DAC and it plugs into the 8255 PPI 26 pin flat cable connector on the single board computer. Ports 'A' and "B' of 8255 are defined in output mode and port 'C' in input mode. The 8 bit data input for DAC 0800 IC is written into the port 'A' output register of 8255 by the CPU. This data can be latched into 74LS373 by applying software generated positive going latching pulse through bit PB0 of port 'B' (used as control port) of 8255 PPI. A logic high state at bit PB0 keeps the latch 74LS373 in flow through condition. When RESET key on board is pressed, the address and data busses of the system as well as the 8255 ports go into tristate

condition, logic 1's by 74LS373 remains in flow through condition, and DAC get's FF Hex as input data and gives the full scale output.

Port 'C' of the 8255 is used as a input status port and it must not be defined in output mode when DAC -01 card is connected to single board computer.

The DAC-0800 gives complementary sinking current output Io and Io proportional to the digital data input and reference voltage. The full scale output current FS for all logic states is given by

$$I_{FS} = Io + Io = (Vref * 255)/(Rref*256)$$

DAC 0800 will give the output full scale current,

$$I_{FS} = Io\ (Vref*255)/(Rref*256)$$

Precision metal film register with high temperature stability are provided for positive and negative references and the reference voltage is variable between 0 to +Vc and are buffered. The output current Io of the DAC-0800 is converted into voltage Vo by precision op amp based current to voltage converter shown in fig.3.3.1.

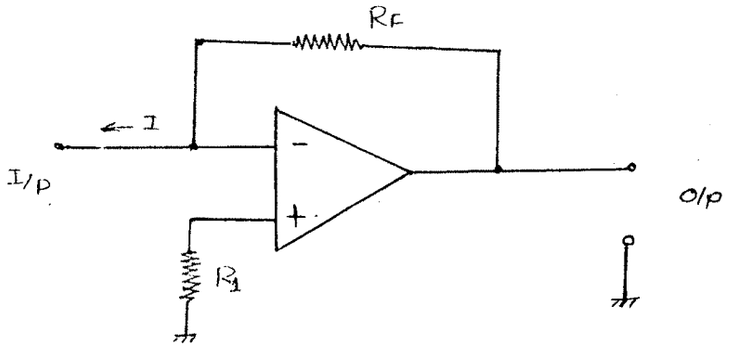


FIG 3.3.1: Current to votage converter.

The current drawn by inverting terminal of op amp is very

small and the current Io sink by DAC-0800 develops a voltage Vo = Io - Rf at the output of the op amp. The output current Io of the DAC-0800 is given by

Io = Vref/Rref(D0/2+ D1/4+D2/8+.....+D7/256)

D_N = 1 if N^{th} data bit is at high state

D_N = 0 if N^{th} data bit is at low state

N = 0 to 7 because DAC is 8 bit.

Since I is sinking current it is negative. So that DAC output voltage is given by

Vo = Vref (Rf/Rref)(D0/2 + D1/4 + D2/8 +.....+ D7/256)

Since I_{FS} is known the value of Rref can be calculated .

Rref = V_{FS}/I_{FS}

Rref = V_{FS}/Io

SYSTEM MEMORY AND INPUT OUTPUT MAPPING :

The system memory is also as important as the CPU itself, because this is where the system program resides and the CPU takes it's instruction from the program. The memory is of two types ROM and RAM. The single board computer has a flexible memory map, and for convenience of program development, the RAM has useful feature such as battery back-up.

MEMORY MAP :

FFFF	USER RAM 6116
C000	EXPANSION
BFFF	EPROM/RAM
4000	MONITOR
3FFF	EPROM

INPUT / OUTPUT MAPPING :

IC	ADRESS	MODE	I/O FUNCTION
8279	04	READ	READ keyboard FIFO
		WRITE	WRITE data to DISPLAY
	05	READ	READ STATUS WORD
		WRITE	WRITE COMMAND WORD
8155	08	WRITE	WRITE COMMAND/STATUS REG.
	09	R/W	PORT A
	0A	R/W	PORT B
	0B	R/W	PORT C
	0C	R/W	TIMER LOW BYTE
	0D	R/W	TIMER HIGH BYTE
8255	10	R/W	PORT A
	11	R/W	PORT B
	12	R/W	PORT C
	13	R/W	CONTROL REG.
8253	18	R/W	COUNTER 0
	19	R/W	COUNTER 1
	1A	R/W	COUNTER 2
	1B	WRITE	CONTROL REGISTER

Programs are described in chapter 4.

CIRCUIT DIAGRAM :

The interface diagram of potential divider shown in fig.3.4. This interface is used along with the program explained in first article of chapter 4 When mode of operation is internal.

CIRCUIT DIAGRAM OF INTERFACING :

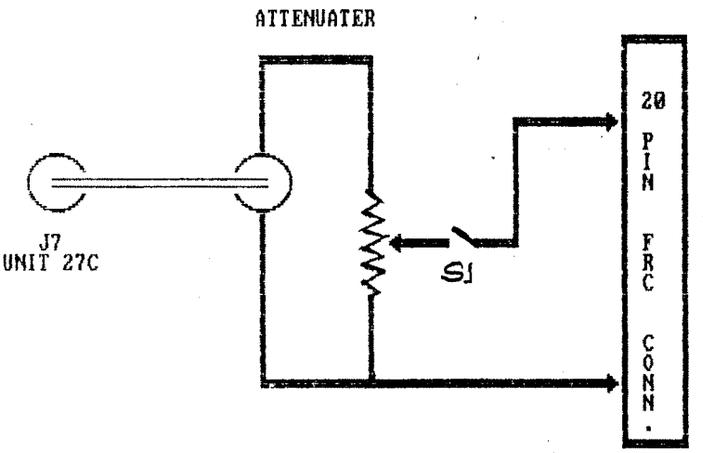


FIG 1 3.4

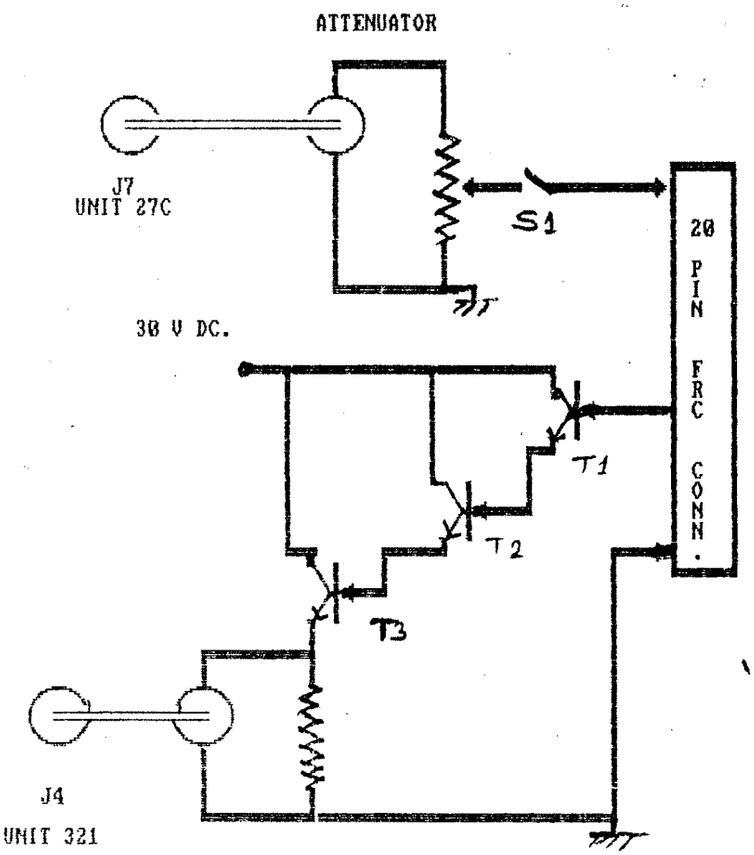


FIG 2 3.5

In the second diagram the pulse derived from PC is amplified through the amplifier stages of T1, T2, and T3. Such that the voltage at output is around 22 V. A pulse is thus connected to J4 of UNIT 321 to trigger the ionosonde and for subsystem externally. The second part of the circuit is as same above in fig.3.4.1. It is used in the second type of operation and explained in chapter 4.

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