C H A P T E R III

HARDWARE DESCRIPTION OF THE KIT.

This chapter is intended to bring out essential features of the kit prototype, assumed while developing monitor software and the interpreter structure, which is suitable for cryophysics laboratories, as described in the previous chapter. Basic theme behind the development of hardware configuration has been to provide a complete form to the software developed, such that it could be tested through emulation on a PC/XT. As described earlier the environment of the microprocessor have already grown richer and it is always possible to select peripheral components, especially the memory modules, with a wide variety of options. The present thesis is limited to accept a viable option than entering into trade-off compar sion of adopting alternative possibilities. Basic CPU configuration and memory mapping have been discussed in the first sub-section. I/O mapping and decode logic are covered in sec. 3.2, while the circuit option to intercouple the kit prototype with a PC/XT are covered in the last sub-section.

3.1. The CPU Configuration And Memory.

The hardware provides two options for getting installed within environment of a PC/XT (or PC in general) viz. a ADD-ON kit or a multimaster[20] slave unit. Further, as outlined in Chapter I, the system is based on a CPU having 8086 as processing

unit. The 8086 has been configured in the maximum mode where the remaining components of configuration are 8284; the system clock generator, 8288; the system bus controller, 3 X 8282 s; octal latches, 2 X 8286 s; the bus transceivers, 8289; the bus arbitrar, is to be installed optionally. For both the options the maximum mode configuration is selected, allowing the same PCB getting converted to suit the requirements of the options. Details of circuit strappings have not been given a full stress at present. Configuration is shown in fig 2.3. This being an adoption of the standard configurations[26,34], discussed throughly in the data sheets, wiring details and functional descriptions of various chips are not covered in the discussion. The fig. 3.1 does not include the bus arbitrar but the configurational details of option the PC ADD-ON are the multimaster slave are discussed in the following sections.

Regarding on-board memory facility, the system offers maximum of 256 KB of memory, where at present the equal weightage is given to the areas, viz. the program area and the object code area, i.e. upto 128 K max for each. The object code area includes the machine code routines defined by the user and the monitor, the interpreter deviced, while tne program area stores the user written program and the data acquised. The present technology offers two options to configure the RAM memory use of static RAMs is recommended for low memory counts, while the higher density dynamic RAM units are prefered for larger memory requirements. Within the configurations 8086, 64 K X 1 dynamic RAM have been

commercially used[35], and total number of 64 dynamic RAM chips would be required to satisfy the present memory requirement. As an alternative using 6164, a 8 K X 8, CMOS technology product, would demand the same chip count and is selected presently to configure the memory. This will definately be a faster choice, through detailed cost and reliability trade-offs are not estimated.

The decode logic is shown in fig. 3.1 (a). Out of the four segments the strapping option is provided to select the segments as 0 - 1, without option, and 2 - 3, ..., E - F by the kit CPU. When the CPU of PC takes charge of kit bus, the object code module area, i.e. segment 2 - 3, ..., E - F, will only be accessible and the decode logic is separate, allowing redefinition of the segment. The decoders are switched either using a derived HLDA output or through a dedicated logic network (sec. 3.3). In PC ADD-ON option the object code memory module will be treated as a I/O device while in the multimaster slave configuration the object code memory module will be a dual port device (sec. 3.3.). The memory of the system as a whole is battery backed and monitor is assumed getting loaded from PC upon an interrupt from the kit, preferably NMI controlled through the keyboard. Further if needed part of the module could be replaced by 2764 units with too little a strapping required.

Logic distribution of memory is given in the table 3.1 and is self explanatory. Fig. 3.1 (b) shows a block diagram for

introduction of wait states. The basic unit of the block is a 8 bit shift register as required[34]. The same block applies with all the modules to generate on-board or off-board READY signals. This being too popular a option is not elaborated at present.

3.2. System I/O And Decode Logic.

The I/O module shown in fig. 3.2 and fig. 3.3 comprises of decode logic, support peripherals including (2 + 2 optional) X 8255 (PPIs), 8279 (KeyBoard and Display Controller), 8251 (USART), 2 X 8254 (PITs), 8259 (PIC), 0808 (ADC), 2 X 8212 for the system use. The module is exclusively for the kit and a 2716 is used as a basic decoder. 8255s and 8279 is decoded directly, where configuration demanded a byte or a word transfer through PPIs. Additionally in combination with DO_5 - DO_7 of 2716 a 74LS138 is used to decode 7 more interface chips. The Table 3.3 shows the address map.

Ports of importance for the software development are discussed below :

1) 8212_1 : It has been used to specify the total memory installed. The chip is in the input mode and informs status of a DIP switch connected to it. The information on the port is decoded in the following Table.

DI3	DI2	DI1	DIO	
x	x	0	0	Not Allowed.
x	x	0	1	64 K.
x	x	1	0	96 K,
x	x	1	1	128 K.
0	0	x	x	Not Allowed.
0	1	x	x	2 PPIs
1	0	x	x	3 PPIs
1	1	x	x	4 PPIs

2) PPIs : The default mode setting of 8255s are as below :

PPI_1 : MODE_0 ; PORT_A, _B, _C as INPUT_PORT.

PPI_2 : MODE_0 ; PORT_A, _B, _C as OUTPUT_PORT.

PPI_3 (Optional) : MODE_1; PORT_A, _CH, INPUT_PORT, PORT_B, _CL OUTPUT_PORT.

PPI_4 (Optional) : MODE_0; PORT_A, _CH, INPUT_PORT, PORT_B, _CL OUTPUT_PORT.

3) PIT_1 : The default mode setting of 8254 is as below :

COUNTER_1 : MODE_3, with BCD counting and the counter loaded with 1000 as the count.

COUNTER_2 : MODE_3, with BCD counting and the counter loaded with 0080 as the count.

System clock has been inputted to COUNTER_1 (C_1) while output of C_1 is connected to CLK of C_2 to generate a square wave of 1 KHz and is inputted to C_0 in MODE_0 to generate interrupt on the terminal count.

4) ADC : The address selection itself selects the channel. Further installation of PGDA[36], LF356 buffers and additional demultiplexers to provide desired pre-amplification and high input impedance is possible. In this situation instead of ADC 0808, ADC 0800 will be employed. These interfaces are throughly discussed in OEM systems book[37].

5) KeyBoard and Display Interface : This unit comprises 8279 as programmable controller. The device is selected to operate Hz and in 2 key roll over encoded scan mode. The display unit is in the left entry typewriter mode. Rest of the circuit configurations are too standard and the key codes corresponding to the various keys are given in Table 3.4.

Remaining features of I/O interfaces are transparent in the fig. 3.2 and fig. 3.3.

3.3. : Options For PC Interfacing.

Fig. 3.4 and fig. 3.5 elaborates the PC ADD-ON interface and multimaster configuration respectively. The PC ADD-ON interface uses a 8212 in the control of PC to communicate HOLD signal and the segment addresses required. Further the same port provides enables to the buffers for address, data and control signals. The service is demanded via an interrupt request from the kit, through 8212_2. A area in object code module of memory could be used for information and parameter transfer to the PC to decide the course of action to be executed. Using this information DMA

transfer will be executed by PC for the data transfer. Further elaboration on the .COM software needed to realise the interface is awaited.

Regarding the multimaster configuration at present we propose to replace 8088 of PC by a PCB, incorporating the multi bus termination. Further the board possesses a logic to acquire a system bus control and managing DMA transfers their_next. The PC will be the master unit while the remaining kits will be the slaves. The bus arbitration logic leaves highest priority to the master. The inter-board communications is always through PC. The strategies adopted for selecting the parameters for data transfer at the level of PC ADD-ON option will be valid in this configuration also.

Table 3.1 : Logical Distribution of Memory.

```
     0000
      :        INTERRUPT TABLE (64 INTERRUPT LEVELS)
     00FF
     0100
      :        DISPLAY ENTRY TABLE (256 BYTES).
     01FF
     0200
      :        DIT
     02FF
     0300
      :        PIT
     03FF
     0400
      :        CONVERT OFFSET TABLE (16 LEVELS).
     041F
     0420
      :        INTERMEDIATE PARAMETER TABLE
     045F
     0460
      :        DATA REFERENCE TABLE.
     047F
     0480 <-.
      :      |  DATA ARRAY AREA (LRN MODE ONLY)
     04DF    |
      :      |> LNO TABLE (RUN MODE ONLY)
     057F <-'
     0580
      :        KB BUFFER
     05AF
     0580
      :        DISPLAY BUFFER
     061F
     0620
      :        USER STACK
     06FF
     0700
      :        RAM BUFFER
     0EFF
     0F00
      :        OFFSET TABLE
     0FFF
.-> 1000       IC CODES
|    |
|
|
|    |        DATA
`-> XXXX       DECIDED BY CONFIGURATION SWITCH.
```

Table 3.2 : Logical Distribution of Memory. (Contd.)

0420 : : 042D	LOCATIONS TO BE LOADED WITH FIXED VALUES
042E : : 045F	LOCATIONS TO BE RESETTED AND VARIABLE PARAMETERS GETTING LOADED AT THE EXECUTION TIME.

The locations are specified in the listing enclosed.

Table 3.3 : I/O PORT ADDRESS MAP

Hex Address	BHE	I/O PORT	Device
FF80H	1	PORT_A	PPI_1,(8255)
FF82H	1	PORT_B	
FF84H	1	PORT_C	
FF86H	1	PORT_CONTROL	
FF81H	0	PORT_A	PPI_2,(8255)
FF83H	0	PORT_B	
FF85H	0	PORT_C	
FF87H	0	PORT_CONTROL	
FF80H	0	PORT_A	PPI_1 & PPI_2
FF82H	0	PORT_B	
FF84H	0	PORT_C	
FF86H	0	PORT_CONTROL	
FF90H	1	PORT_A	PPI_3,(8255)
FF92H	1	PORT_B	
FF94H	1	PORT_C	
FF96H	1	PORT_CONTROL	
FF91H	0	PORT_A	PPI_4,(8255)
FF93H	0	PORT_B	
FF95H	0	PORT_C	
FF97H	0	PORT_CONTROL	
FFA0H	1	R/W KBDC DISPLAY RAM OR READ KBDC FIFO.	KBDC (8279)
FFA2H	1	READ KBDC STATUS OR WRITE 8279 COMMAND.	

Hex Address	BHE	I/O PORT	Device
FFB1H	0	COUNTER_0	PIT_1 (8254)
FFB3H	0	COUNTER_1	
FFB5H	0	COUNTER_2	
FFB7H	0	CONTROL_REG	
FFB0H	1	COUNTER_0	PIT_2 (8254)
FFB2H	1	COUNTER_1	
FFB4H	1	COUNTER_2	
FFB6H	1	CONTROL_REG	
FFC1H	0	DATA_PORT	8212_1
FFC0H	1	CONTROL_WORD	PIC (8259)
FFC2H	1		
FFD1H	0	R/W DATA_PORT	USART(8251)
FFD3H	0	READ 8251 STATUS, WRITE 8251 CONTROL	
FFD0H	1	ADC CH_0	ADC 0808
FFD2H	1	ADC CH_1	
:			
FFDEH	1	ADC CH_7	
FFE1H	0	DATA_PORT	8212_2

Table 3.4 : Key Codes Of The Keys Used.

KEY MNEMONIC	HEX CODE	KEY MNEMONIC (FUNCTION)	HEX CODE
0	00	CH	3C
1	01	CNVRT	40
2	02	RET	44
3	03	DLY	48
4	04	OUB	4C
5	05	INB	50
6	06	INW	54
7	07	INR	58
8	08	OUW	5C
9	09	LET	60
A	0A	DCR	64
B	0B	IF	68
C	0C	GSB	6C
D	0D	DSP	70
E	0E	FOR	74
F	0F	GTO	78
.	10	NXT	7C
$	2B	END	81
,	2C	THEN	82
ENTER	2D	AUTO	85
-	2E	LRN	89
+	2F	DAT	8D
*	30	RUN	91
/	31	LST	95
=	32	VAC	99
≠	33	DEL	A1
<	34	EXT	A5
<=	35	NOR	A9
>	36	16I	AD
>=	37	24R	B1
KB	38	--	--

KEY MNEMONIC (REAL VARIABLE)	HEX CODE	KEY MNEMONIC (INTEGER VARIABLE)	HEX CODE
A	11	Q	21
B	12	R	22
C	13	S	23
D	14	T	24
E	15	U	25
F	16	V	26
G	17	W	27
H	18	X	28
I	19	Y	29
J	20	Z	30
K	21		
L	22		
M	23		
N	24		
O	25		
P	26		

KEY MNEMONIC (CURSOR)	HEX CODE
-->	3A
<--	3B
I	3D
i	3E

FIG 3.1 DECODE LOGIC AND MEMORY MODULE A, B,

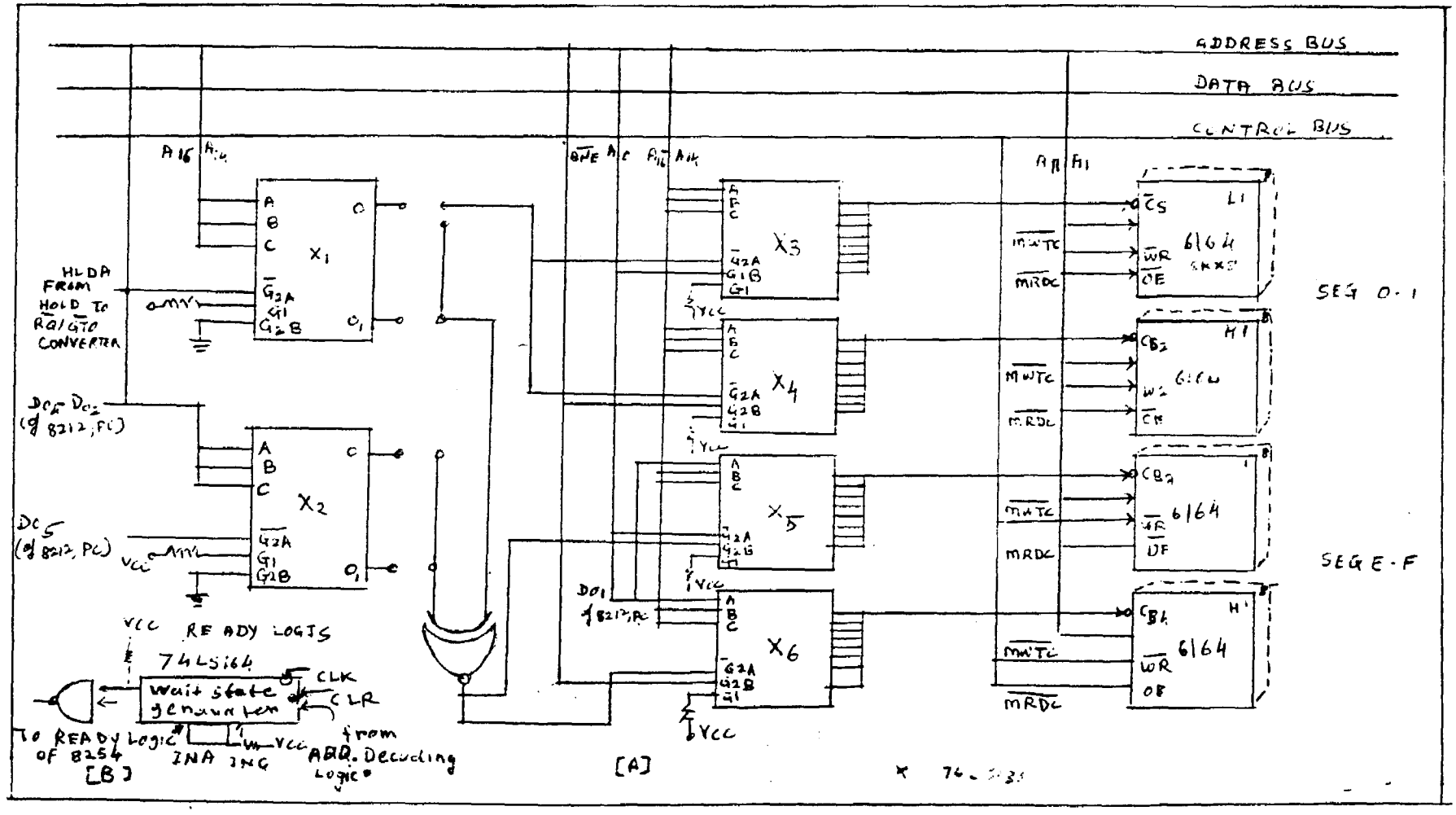

FIG 3.2 B I/O DECODE AND PERIPHERALS

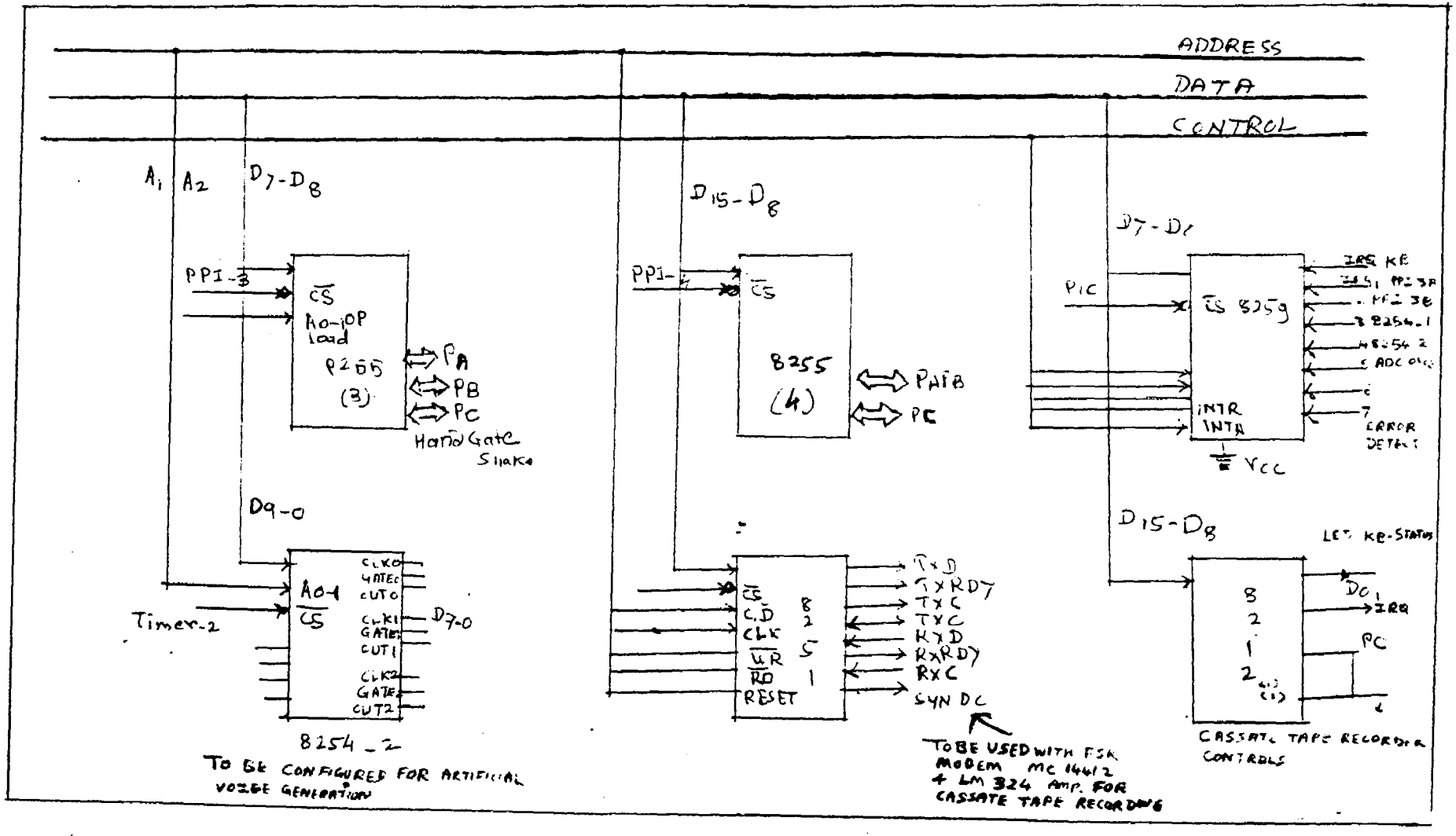

FIG 3.3 ABC ADC, KEYBOARD INTERFACE & ANALOG INPUT INTERFACES

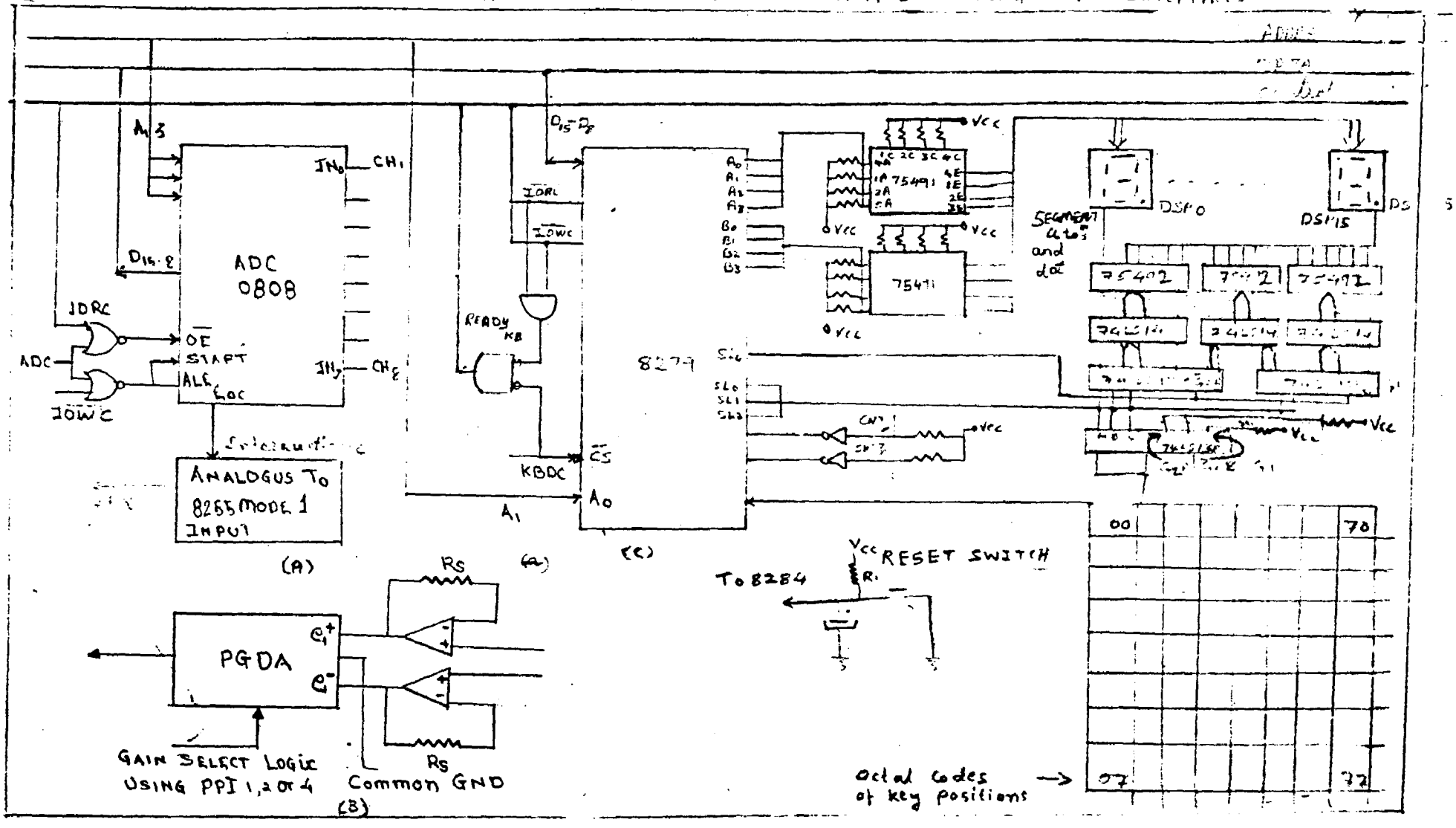

Fig 3.4 PC ADD-ON INTERFACE

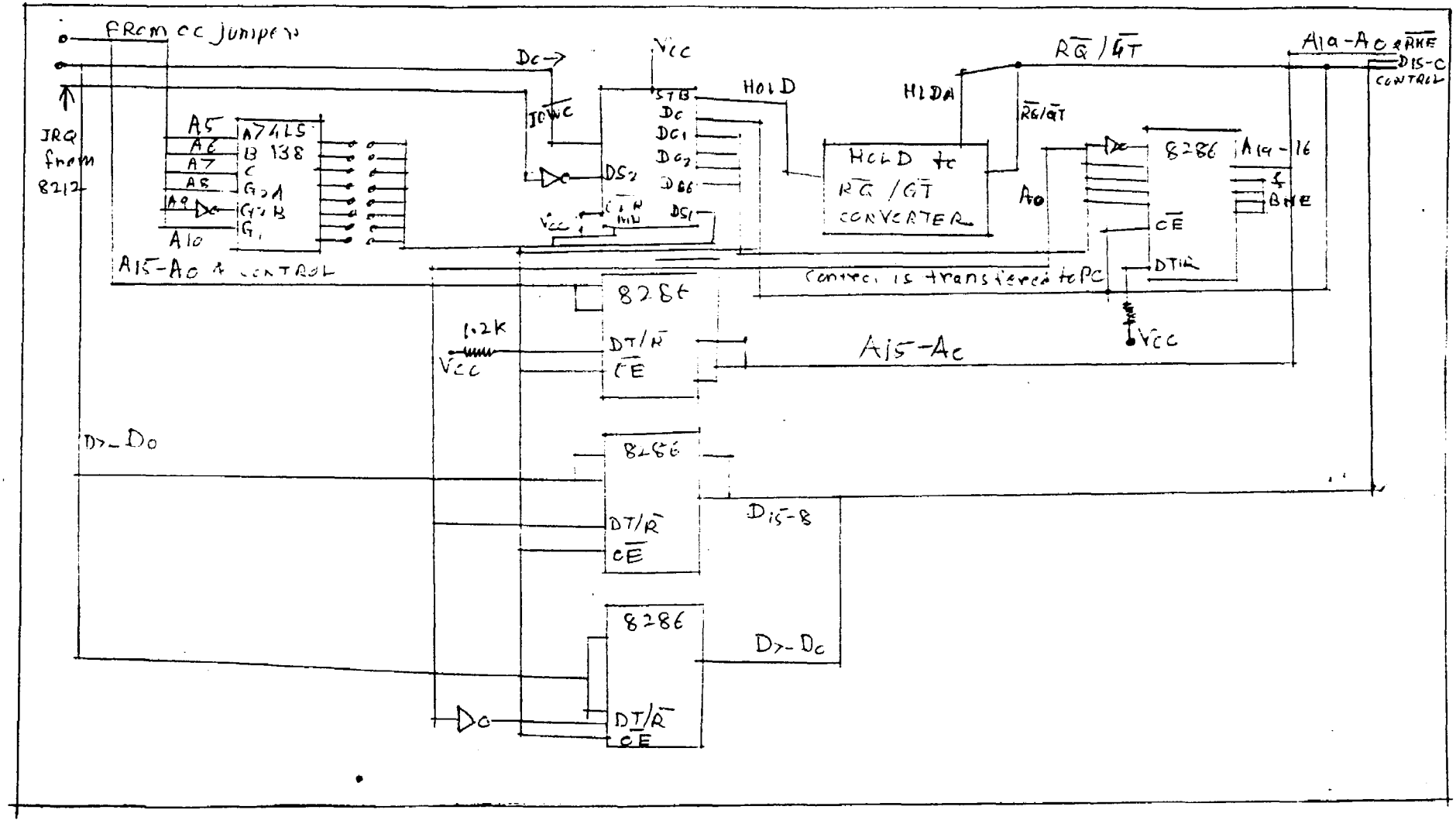

FIG 3.5 MULTI MASTER SLAVE INTERFACE