

List of Figures

- 2.11 Block Diagram of Analog Scope
- 2.12 Block Diagram of DSU
- 2.13 Cursor Display
- 2.14 Interpolation Techniques
- 2.15 Random Sampling
- 2.16 Equivalent Sampling
- 2.21 Standard Test Load for Toem-pole Output
- 2.22a Waveforms of Inverting & Noninverting Functions
- 2.22b Set & Hold Time on Rising Edge of Clock
- 2.22c Set & Hold Time on Falling Edge of Clock
- 2.22d Propagation Delay from Rising Edge of Clock
- 2.22e Propagation Delay from Falling Edge of Clock
- 2.22f Propagation Delay from Set & Clear
- 2.22g 3-State Output Low & Enable Disable Time
- 2.22h 3-State Output High & Enable Disable Time
- 2.22i Setup and Hold Time to Active Low Enable for Parallel Load
- 2.22j Setup and Hold Time to Active High Enable for Parallel Load
- 2.23 Graph of tpd against C (C load)
- 2.24 Graph of tpd against t (Ambient temperature)
- 3.11 Block Diagram of HM203 Oscilloscope
- 3.12 Block Diagram of DSO Interface
- 3.13 WR Timing for 2148L
- 3.14 RD Timing for 2148L
- 3.30 Clock Generation Circuit
- 3.31a Slow Mode Address Generator
- 3.31b Slow Mode Address Generator, Timing
- 3.32 Synchronous Reset Generator
- 3.33a Fast Mode Address Generator
- 3.33b Secondary Counter Alternate TCu Timing
- 3.33c Trigger Mark Timing
- 3.33d RST 7.5 Delay Timing
- 3.34a Repeatative Mode Address Generator
- 3.34b ECL Clock & Repeatation Mode Acquisition Timing
- 3.34c Address Multiplexing with Slot
- 3.34d Repeatative, Display Mode Address Generator
- 3.35 Display Circuit
- 3.36 Acquisition Memory Control Circuit
- 3.37 DMA & Memory Control Circuit
- 3.38a Control Circuit for WF
- 3.38b Control Circuit for WE Timing
- 3.39 Channel Select Logic
- 3.39a Up Start Control Circuit
- 3.41 UA 733 Amplifier Section of HM203
- 3.42 Synchronous Reset Generator (Testing Circuit)
- 4.21 up Interface Schematics, Intel 8085
=====