CHAPTER - I

CHAPTER - 1

INTRODUCTION

A few years back, M/s.Tektronics, Inc. was doubtlessly considered as trend setters in the oscilloscope technology in specific and sophisticated display terminal technology in general. Tectronics had offered the analog oscilloscope with bandwidth upto 1GHz. It had launched two series of digital storage oscilloscopes, viz. 2200 and 2400 series (1). Before Hewlett and Packard, has introduced its system HP54503 (2) with 500 MHz real-time bandwidth and simultaneous acquisition of 500 MS/sec on 4 channels of the scope, the Tek-2440 was leading in market of Digital Storage oscilloscopes [DSO]. The Philips offers a system, PM3340 (3) with 10 bits of vertical resolution and has an added advantage of integral signal processing capability. Beyond the normal algebric operations on the real-time signals, the system offers signal comparison and FFT processing. Further the cursor positioning is also automatic. To name a few more companies in the DSO field are Iwatsu (4), LeCroy (5), Nicolet (6) etc.

Jonah, McLeod has analysed out burst of the DSOs in the market (7) and coated a remarkable rise in the sales of DSO at 30% during last five years. The advanet in the computer technology, memory technology [Availability of 4K X 1 to 8K X 8 SRAMs, upto 20 nsec access time], and semiconductor technology in general [Availability of wide variety of ADC, flash converters and DAC at video speeds] (8) has definately contributed to the fast growing market of DSOs. Availability of RAMs at cheaper rate, interfacing

capability of DSO to any computing system makes DSO a signal processing tool than being a simple waveform display system (9).

The discussion of market status and availability of the DSOs is mainly oriented to emphasize the shift of thrust on devicing technologies to implement digital processing techniques in those areas whichever were thought to be the purview of analog processing (7). For the chronological review of the technology implemented in DSOs a reference is made to a few articals in electronics (10, 11, 12). The recent technology based on ECL logic [A/D converters at 5 nsec sampling time] and P^2CCD technology by `Philips' (13) made 500MS/sec and 1 to 2 GHz band-width a feasible choice.

As far as the circuit features of analog and storage oscilloscopes are concerned, the difference lies at the level of intermediate amplifier and trigger generation modules. Inherently the trigger generation and storage controls available upon trigger are the lucritive features of the DSOs (14). Though at present the market thrust is towards making the DSOs capable of signal processing, required in general in the communication technology (15, 16), imaging system in medical instrumentation etc., there exist a wide range of applications where the requirements of signal processing and interaction of sampling with trigger is characteristically different from that of the available DSOs. Mainly we want to point out to the requirement of smart data acquisition and signal processing systems dedicated for the analytical instruments. Analysis of these requirements and

estimate of suitability of DSO, in these fields does not form the topic for the present discussion, but the statement is not an ad-hoc one.

The analog oscilloscopes available in the laboratory could be coupled to an interface such that it would become a DSO. As approximately 50% of the circuit cost would be common for both the analog and digital storage oscilloscopes, such an interface would add a DSO at lesser cost to the laboratories. In the Indian market M/s.Scientific Instruments Company has very recently came up with a system HM205-2 with 5MS/sec acquisition speed and 20 MHz real-time bandwidth (17). The HM205-2 costs approximately Rs.45,000/-. The interface we propose is roughly estimated to cost nearly Rs.10,000/- or less. It adds the advantages of 10MS/sec sampling speed and various triggering modes not offered with HM205-2. Neverthless, the cost comparison is not the sole criteria for the utility of the proposed project.

Salient features of the interface and the topic of dessertation is as below. It is concerned with defining, designing and testing partly a versatile interface to a 20MHz analog scope to convert it in to a DSO. Input attenuator stage of any analog oscilloscope has impedance matching networks coupled with a FET or any high input impedance buffer/pre-amplifier. Variable voltage preset controls, AC/DC input conditioning is also accomodated in the same stage. These stages amplify the input signal and generate a symmetric and bound voltage signal proportional to the deflection in cms, thus nullifying the effect of V/div settings.

Output of these stages are fed to intermediate amplifier through analog switches. The proposed interface would tap the analog signal at this stage. The channel switching logic will be characteristically different from that of analog oscilloscope, but the trigger generation circuit would be similar. Neverthless, in various modes of operation of the scope the interaction of trigger with the data acquisition/storage process and the display of the stored information will be characteristically different, for the DSO interface. Unlike the analog counter part the acquisition and display would be treated as two different events and therefore the actual hold-off time encountered in these systems will be sufficiently large, except in case of too slow time base settings. Further, to reconsile with auto and normal modes of the action, Add/Chp/Alt controls, trigger on Ch_1, Ch_2 and increased activity of the scope with reference to the trigger, the requirement of greater interrupt vectoring will be needed for the interface. At present we propose to build the system around processor Intel 8085 for the reasons elaborated in Sec.2.3. Further we consider the experience of design of such a system would definately be benificial for the development of smart and intelligent data acquisition/display system for the analytical instruments, as discussed in the previous para. Design of such a system is our real interest and the project may be extended for the same purpose.

Layout of the dissertation is as below -

1) The Chapter No.2 is ment to discuss the DSO technology where the emphasis is on available sampling and data acquisition techniques to accomplish acquisition of signal at frequencies beyond 2/sampling rate [alising limit] (14). Further various features of ECL and TTL design, relevant to high frequency design, are also discussed. Survey of the microprocessing capabilities, processing requirements of the DSO and the techniques of software test/development also form part of the discussion in Chapter 2.

2) The Chapter No.3 unveils the hardware circuits of the interface, the overall block diagram is discussed first. The individual modules within the block are elaborated. Consequently, a attempt is also made to specify various modes of operation and software interaction intended.

3) The Chapter No.4 elaborates the software design along with the detailed mapping. The software techniques used to execute operations within each proposed mode are also discussed. The Chapter is added with the machine language and opcode listing of the software designed.

4) Chapter 5 resumes the achievements of the project.