CHAPTER - III

CHAPTER - 3

DIGITAL STORAGE OSCILLOSCOPE

3.1. DIGITAL STORAGE OSCILLOSCOPE INTERFACE :

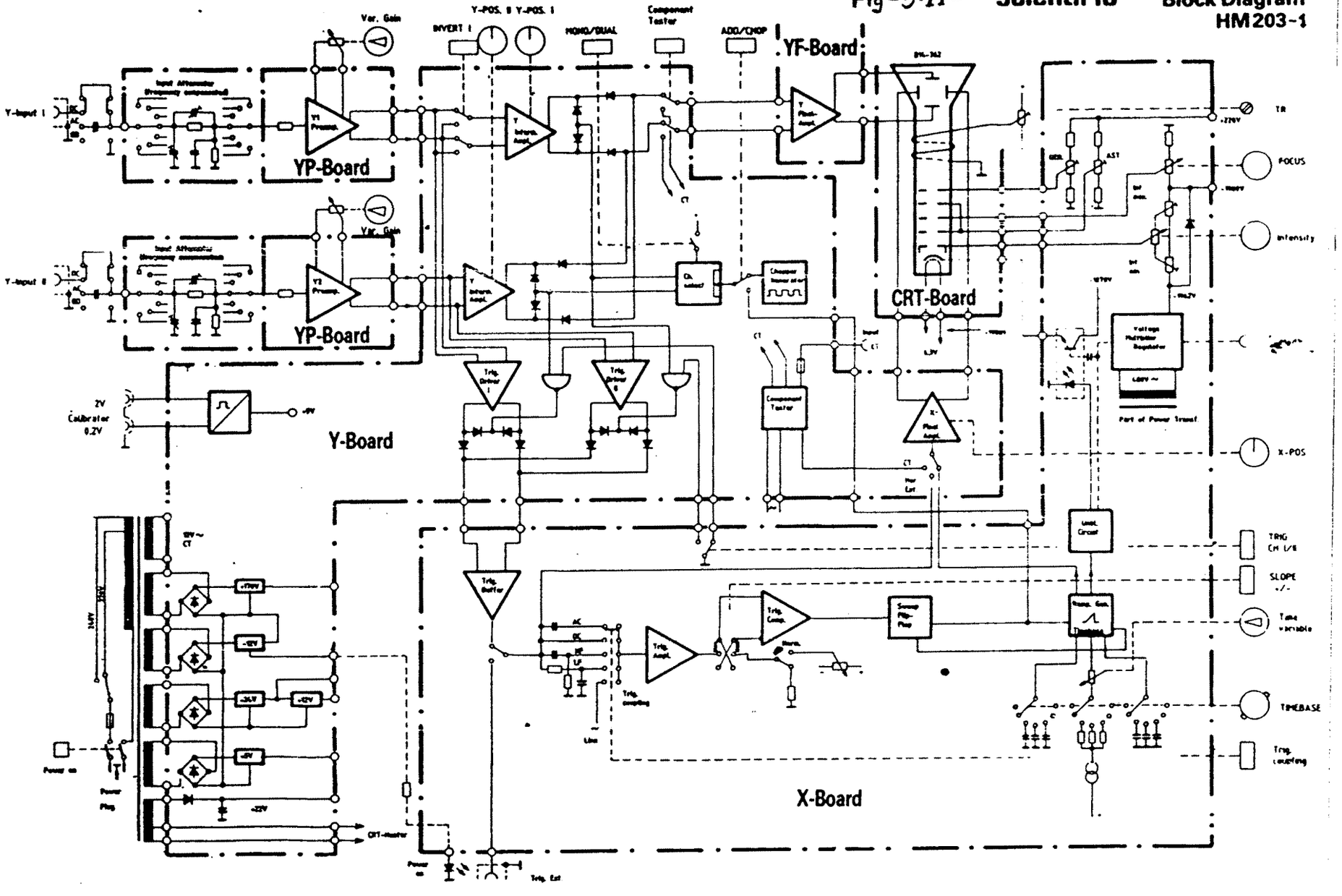
The block diagram of the analog scope [HM 203 model of Scientific] and the block diagram of digital storage oscilloscope [DSO] interface with conventional analog oscilloscope [HM 203 model of Scientific] is given in Fig. 3.11 and 3.12 respectively. Neverthless, conceptually the interface would be applicable to any analog scope operating within 20 MHz real time bandwidth.

The scope work as an analog scope, if the interface card is absent and the identity of it does not change. Upon incertion of interface card, the data selector switches select the digital storage operation mode. The data selector logic is powered using the power supply of analog scope itself.

To develope overall insight in the operation of the DSO interface proposed, functicnal existance of each block has been given in block diagram 3.12 below.

i) The Memory Storage Unit : The unit accomodates two blocks of 2K RAM memory organised to store data acquised from `Ch-1' and `Ch-2' respectively and are refered as `Mch1' and `Mch2' respectively. The memory unit is configured out of NMC2148L / NMC2148-3 chips, [4 X 1K] NMOS static RAMs with access time of 55 nsec (33). The requirement is because of 10 MS/sec acquisition speed proposed. The memory unit is accessible to both 1) DSO interface operating

Fig-3·11- scientific Block Diagram HM203-1



with dedicated data acquisition, storage and display logic units and 2) the microcomputer controlling the overall operation. Data path selector, buffers, transivers are appropriately used to effect the memory sharing. The word length of the memory is of 9 bits, out of these 8 bits are used to store the amplitude of the signal, while the 9th bit stores the cursor and trigger information.

ii) Analog to Digital Converter Interface : It's heart of the DSO. Analog input appears to the converter from the pre-amplifier/attenuator block of the analog scope and thus does not alter the input impedance of the scope interfaced. The signal is appropriately amplified/level shifted, to match the requirements of the analog to digital converter [ADC]. The ADC proposed is CA3308, which is a 8 bit flash converter, employing parallel convertion technique (Sec.2.1). The minimum conversion time offered is 66 nsec. The device optionally converts analog signals on high or low outputs of the reference clock. The device is used in the option of high phase of the clock and thus a pulse of 50 nsec is sufficient to acquire and convert the sample. The scheme has allowed us to avoid any kind of sample and hold circuits. No doubt we expect signals of low repetition rates (Sec.21). The pulse repetition rate of the ADC conversion clock is varied in relation to the time base setting to acquire 1024 samples per horizontal frame.

iii) Clock Generator : The clock generator uses basic clock of 20MHz, to generate clock of 50 nsec pulse width and variable duty cycle. The duty cycle depends upon time base settings. The clock

frequency is managed such that 1024 clock pulses appears per screen width treated as 10 cms. The clock is refered as MSMV or an acquisition clock. A special purpose circuit is deviced to generate MSMV clock of the variable duty cycle. The frequency is controlled by the up latching a divisor count. The MSMV clock is subjected to a few buffer tc generate advanced and retarded clock signals (Sec.3.3).

iv) Address Generators : The mode of storage of the aquised data depends critically upon the time base settings. Two limiting factors are to be taken into consideration. a) The operation of 'Auto' mode and b) The maximum sampling speed. If the auto mode is selected, the trigger generator waits for about 500 msec to recognise no trigger and then generates trigger automatically, therefore for time base setting 0.1 s/div and 0.2 s/div the philosophy of acquisition and storage is characteristically different than the modes with faster sweep rates. Therefore these two time base settings are treated separately as far as mode of storage and display is concerned. The mode of storage dictates the address and read/write control generation and therefore separate circuit block is active in this time base selection. A hardware switch is also provided to increase the effective time base by a factor of ten optionally. Thus providing 1 s/div and 2 s/div time base effects.

For the time base settings between 50 ms/div to 10 μs/div, the sampling occurs as a record of 1024 valid events, with a trigger marker mounted in the desired location, to faciliate pre

and post-trigger acquisitions. A separate address generator is proposed in this range.

As the sweep rate is increased further the equivalent sampling technique is to be adopted (Sec.2.1). At present we have opted for the random sampling technique. For the purpose the ECL vernier counter is deviced. The least count of the counter = 2 nsec. Using this counter the slot of data storage is determined and the remaining sampling events store data into these slots. The process is repeated till all the memory locations are filled. The number of repeatations [slot weight] is statistically valid, further the slot weight is software programable also.

Dependent on the range of time base selection up multiplexes the required circuit to generate the address. Address generation of various modes of operations are elaborated separately in the dissertation.

v) $\overline{RD}/\overline{WR}$ Control and Display : Read/Write timings of memory componant 2148L is shown in the Fig. 3.13, 3.14.
Specifications of these cheaps is given in the Appendix.

It is apperant that if a memory chip is selected the data bus would hold the data of the address location selected. Therefore the $\overline{RD}/\overline{WR}$ control pulse required is write enable [$\overline{WE}$] signal only. A monostable multivibrator circuit has been used to provide the required $\overline{WE}$ signal. At the time of data acquisition $\overline{WE}$ is applied to data acquisition memory, while at the time of display or DMA storage [save mode] the $\overline{WE}$ is applied to the output

latch or the DMA memory bank respectively. The address of DMA location is generated by a separate address generator circuit, the 74LS193 acts as output latch.

vi) Information Display : A generalised display circuit to annunciate the ΔV and ΔT, between the cursor locations, and the mode selection menu, at the time of presetting the DSO, is deviced and operates on 20MHz, as the basic clock. Y register is used to position the information vertically and 1024 clock cycles of basic clock scan the horizontal width. The display is of single line only and the vertical register/counters changes between E0 and E8. As many as 32 characters are accomodable in a line. up loads the relevant character in the display RAM [32 X 8] and passes control to the display circuit. Display circuit treats each character code and Y position as an address to the address generator. The address generator feeds it's output to the Z-control of the scope, through an 8 bit shift register. The X and Y position outputs are A/D converted and fed to X and Ch1 final amplifiers respectively. The X and Y counters are physicaly the same in information and data display modes. Upon power on reset the X and Y [Ch1 and Ch2], deflection controls are also reset to position the beam in the centre of the screen.

The encoded X and Y position information is fed to a D/A converter viz. DAC 0800 (Appendix). The level shifting/signal pre-conditioning circuits proposed are similar to those used in the intermediate X, Y amplifier sections of the analog oscilloscope. Therefore are not discussed in detail.

vii) The Save Mode and DMA Operation : If the data acquired is desired to be saved for future comparison, then the DMA facility of the interface could be exploited. If the save mode is selected the scope is constrained to operate in mono mode only. Upon single acquisition cycle, the data acquired, properly positioned with respective to the cursor, is transfered to one out of four save memory banks. The selection of memory bank is through menu. In save display mode the saved information could be displayed as one of the channels. The only constraint on the display of saved data is that the display can not occure in the chop mode, if dual mode is selected.

viii) Multiplexing and Control : Operation of DSO in various modes is controlled through the up. Up is meant to select Mono/Dual, ALT/CHP modes of operations. Further up provides chip select to the desired memory bank relevant with the operating modes. Additionally it selects the proper data path. It is responsible for providing the clock of the required duty cycle and selecting the relevant address generation mode. The up outputs a control signal to a circuit which synchronises the operations of acquisition, the address generation. $\overline{RD}/\overline{WR}$ control generation and display of signal and information with the acquisition clock. All these activities of up are software controlled. The software control is elaborated in the next chapter.

3.2. AVAILABLE MODES OF OPERATION :

It is worthwhile to reasset that the activities upon trigger of DSO and that of its analog counter part, differ

drastically from each other. If the interface is mounted the up annunciates for mode setting [For details reference is made to Chapter 4]. The up sorts out the mode of operation as far as the DSO is concerned. A acquisition cycle, a display cycle or a save information cycle is an individual activity. Up sets proper commands sequentially to execute the desired over all operation. The various activities of the DSO are given in the Table 3.21, the modes which are not available with analog scope, being out product of the DSO interface, are marked with asterick (*).

Table 3.21

Available Modes of Operation

Sr. No.	Available Modes	Control Word	Action No.	Remark
1.	Slow-Mo-Ch1 (T) Acq.*	1,0A H	01	Updates the Acq.& Disp for 1K samples on Ch1
2.	Slow-Mo-Ch2 (T) Acq.*	1,05 H	02	Updates the Acq.& Disp for 1K samples on Ch2
3.	Slow-Mo-Ch1 (U) Acq.*	1,2A H	03	Updates the Acq.& Disp from left to right continuously on Ch1
4.	Slow-Mo-Ch2 (U) Acq.*	1,25 H	04	Updates the Acq.& Disp from left to right continuously on Ch2
5.	Slow-Du-CHP-Ch1 (T)*	1,CA H	05	Updates the Acq.& Disp for 1K samples in CHP mode for trigger on Ch1
6.	Slow-Du-CHP-Ch2 (T)*	1,C5 H	06	Updates the Acq.& Disp for 1K samples in CHP mode for trigger on Ch2
7.	Save Disp-Slow-Mo-Ch1	1,18 H	07	Display the stored data on Ch1, saveflag is set

Sr. No.	Available Modes	Control Word	Action No.	Remark
8.	Save Disp-Slow-Mo-Ch2	1,14 H	08	Display the stored data on Ch2, saveflag is set
9.	Save-Slow-Mo-Ch1	1,02 H	09	Save the 1K samples acquised on Ch1, saveflag is set.
10.	Save-Slow-Mo-Ch2	1,01 H	0A	Save the 1K samples acquised on Ch2, saveflag is set.
11.	Save Disp-Fast-Mo-Ch1	2,18 H	0D	Display the stored data on Ch1, saveflag is set
12.	Save Disp-Fast-Mo-Ch2	2,14 H	0E	Display the stored data on Ch2, saveflag is set
13.	Save-Fast-Mo-Ch1	2,02 H	0F	Save the 1K samples acquised on Ch1, saveflag is set.
14.	Save-Fast-Mo-Ch2	2,01 H	10	Save the 1K samples acquised on Ch2, saveflag is set.
15.	Save Disp-Rept-Mo-Ch1	3,18 H	11	Display the stored data on Ch1, saveflag is set
16.	Save Disp-Rept-Mo-Ch2	3,14 H	12	Display the stored data on Ch2, saveflag is set
17.	Save-Rept-Mo-Ch1	3,02 H	13	Save the 1K samples acquised on Ch1, saveflag is set.
18.	Save-Rept-Mo-Ch2	3,01 H	14	Save the 1K samples acquised on Ch2, saveflag is set.
19.	Fast-Mo-Ch1 Acq.	2,0A H	18	Updates the acq. for 1K samples from trigger on Ch1.
20.	Fast-Mo-Ch1 Disp*	2,02 H	19	Display the acquised data on Ch1.

Sr. No.	Available Modes	Control Word	Action No.	Remark
21.	Fast-Mo-Ch2 Acq.	2,05 H	1A	Updates the acq. for 1K samples from trigger on Ch2.
22.	Fast-Mo-Ch2 Disp*	2,01 H	1B	Display the acquised data on Ch2.
23.	Fast-Du-ALT Ch1 Acq.	2,8A H	1C	Updates the acq. for 1K samples from trigger on Ch1 in ALT mode.
24.	Fast-Du-ALT-Ch1 Disp*	2,92 H	1D	Display the acquised data on Ch1 in ALT mode
25.	Fast-Du-ALT-Ch2 Acq.	2,85 H	1E	Updates the acq. for 1K samples from trigger on Ch2 in ALT mode.
26.	Fast-Du-ALT-Ch2 Disp*	2,91 H	1F	Display the acquised data on Ch2 in ALT mode
27.	Fast-Du-CHP-Ch1 Acq.	2,CA H	20	Updates the acq. for 1K samples from trigger on Ch1 in CHP mode.
28.	Fast-Du-CHP-Ch1 Disp*	2,D2 H	21	Display the acquised data on Ch1 in CHP mode
29.	Fast-Du-CHP-Ch2 Acq.	2,C5 H	22	Updates the acq. for 1K samples from trigger on Ch2 in CHP mode.
30.	Fast-Du-CHP-Ch2 Disp*	2,D1 H	23	Display the acquised data on Ch2 in CHP mode
31.	Fast-Mo-Add-Ch1 Acq.	2,4A H	24	Updates the acq. for 1K samples from trigger on Ch1 in Add mode.
32.	Fast-Mo-Add-Ch1 Disp*	2,52 H	25	Display the acquised data on Ch1 in Add mode
33.	Fast-Mo-Add-Ch2 Acq.	2,45 H	26	Updates the acq. for 1K samples from trigger on Ch2 in Add mode.
34.	Fast-Mo-Add-Ch2 Disp*	2,41 H	27	Display the acquised data on Ch2 in Add mode

Sr. No.	Available Modes	Control Word	Action No.	Remark
35.	Rept-Mo-Ch1 Acq.	3,0A H	28	Updates the acq. for 1K samples from trigger on Ch1.
36.	Rept-Mo-Ch1 Disp*	3,02 H	29	Display the acquised data on Ch1.
37.	Rept-Mo-Ch2 Acq.	3,05 H	2A	Updates the acq. for 1K samples from trigger on Ch2.
38.	Rept-Mo-Ch2 Disp*	3,01 H	2B	Display the acquised data on Ch2.
39.	Rept-Du-ALT-Ch1 Acq.	3,8A H	2C	Updates the acq. for 1K samples from trigger on Ch1 in ALT mode.
40.	Rept-Du-ALT-Ch1 Disp*	3,92 H	2D	Display the acquised data on Ch1 in ALT mode
41.	Rept-Du-ALT-Ch2 Acq.	3,85 H	2E	Updates the acq. for 1K samples from trigger on Ch2 in ALT mode.
42.	Rept-Du-ALT-Ch2 Disp*	3,91 H	2F	Display the acquised data on Ch2 in ALT mode

Note : The format for the control word is as below.

Mode Du/$\overline{Mo}$ CHP/$\overline{ALT}$ U/$\overline{T}$ or N/$\overline{A}$ D/$\overline{A}$ Ch1 Ch2 MCh1 MCh2

Slow = 01 H, Fast = 10 H and Rept = 11 H

After these individual activities are executed in proper sequence, the resulting modes of operation at the user level are as below.

a) The Save Mode : This mode is operative if the scope is set in to the mono mode. The up performes the acquisition cycle [i.e. acquisition and display cycle in slow mode] and then saves the

information acquired in the memory bank specified. The system returns to monitor after storage. The activity sequence performed in this mode is exemplified below.

Example 1 : Save Mode (Trigger) Ch1

The sequence is 1, 9, 0, returns to the monitor.

Example 2 : Save Mode (Untrigger) Ch2

The sequence is 4, 10, 0, returns to the monitor.

b) Acquisition + Display Mode : The activity of analog and the DSO is almost the same in this mode. In the slow and repetitive modes the trigger is always positioned at the left most corner. Conversely, in the fast mode triggers are allowed anywhere on the screen. The Auto/Normal mode of operation is reconciled through the software only. In this mode the repeatition sequences are not very straight forward, a few examples are given below -

Example 1 : Acq+Disp (Auto) Ch1

The sequence is 19, 19, ..., 20, 19, 19 ...., 20, and so on. The number of repeatition of acquisition depends upon time base setting.

Example 2 : Acq+Disp (Normal) Ch2

The sequence is 21, 22, 21, 22, ... and so on.

The acquisition is discarded until trigger is received.

c) Save Display Mode : In this mode the signals saved in the save mode are displayed on the specified channel. In the mono mode the information appears on the channel selected. While in dual [ALT] mode the information appears on the channel not selected from the pannel. Further in dual mode, before the display of the saved information, acquisition and display cycles of the channel

specified are executed. The time base at the time of acquisition does not keep any relevance at the time of display, therefore this mode could be used to acquire information at slow speed and display it at a higher speed such that persistance of vision will not pose any visual constraint. In this mode the action sequences are in the following manner.

Example 1 : Save-Disp (Mono) Ch1

The sequence is 7, 7, ..., and so on.

Example 2 : Save-Disp (Dual) Ch2

The sequence is 25, 26, 11, 25, 26, 11, ... and so on.

The Ch2 is acquised and displayed directly and the stored data is displayed on Ch2 as in ALT mode.

All the numbers in the examples given above refer to serial number in Table 3.21.

3.3. DISCUSSION OF INDIVIDUAL CIRCUIT BLOCKS :

1) Slow Mode Address Generator : The basic unit generating the address output is a 12 bit counter configured using three 4 bit Hex, Up/Down counters 74LS193 [The data sheet corresponding to the IC has been reproduced in Appendix] 10 LSBs of the counter are used for providing the address to the memory, while the 11th bit acts as an edge triggered interrupt to indicate end of acquisition of 1K samples. The features of control circuit for the address generation are as below. The circuit schematic and timing diagram in slow mode are shown in Fig. 3.31a, 3.31b [Rising and falling edges of the digital signals are shown as vertical lines for convenience, in all the timing diagrams].

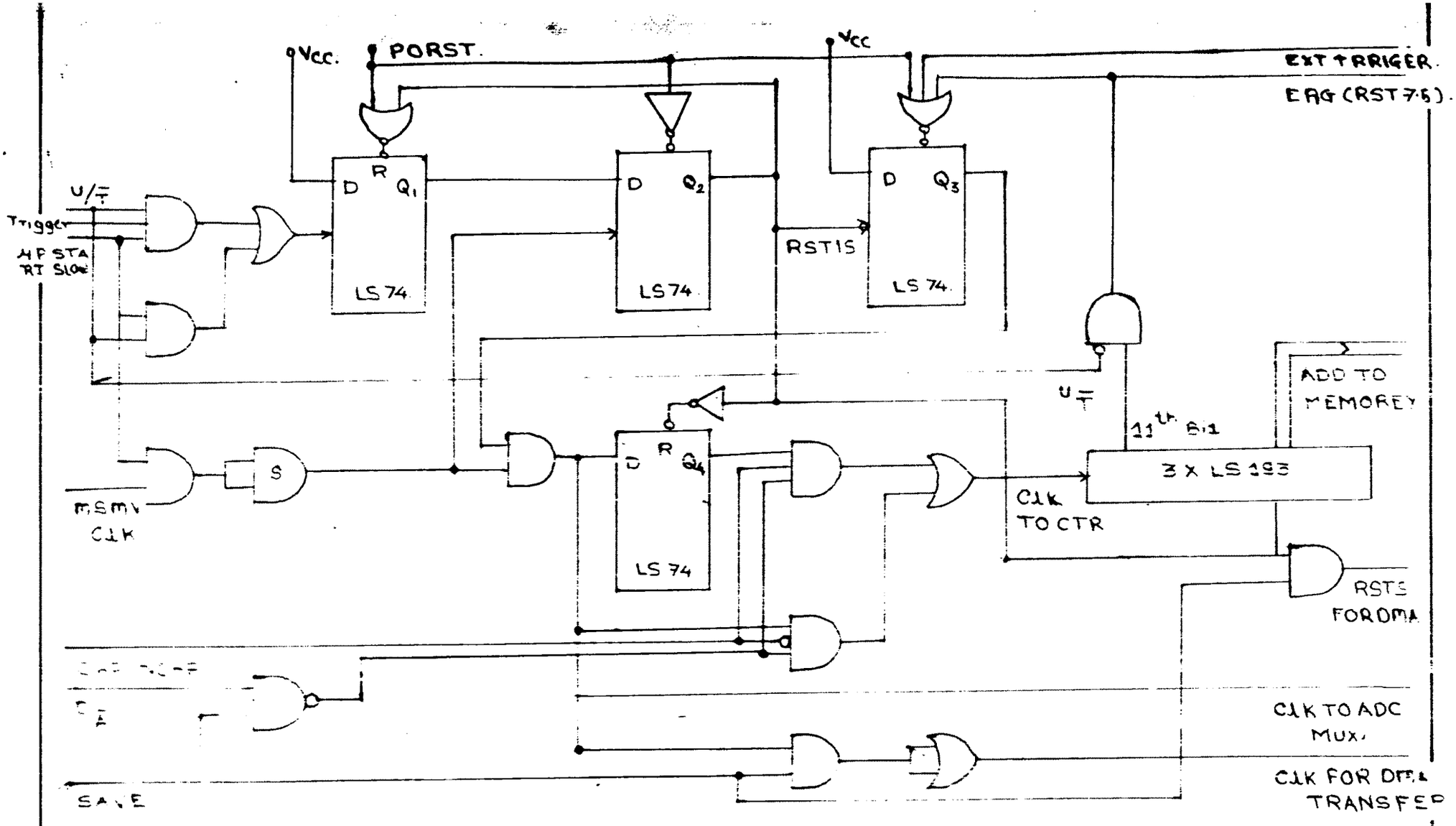
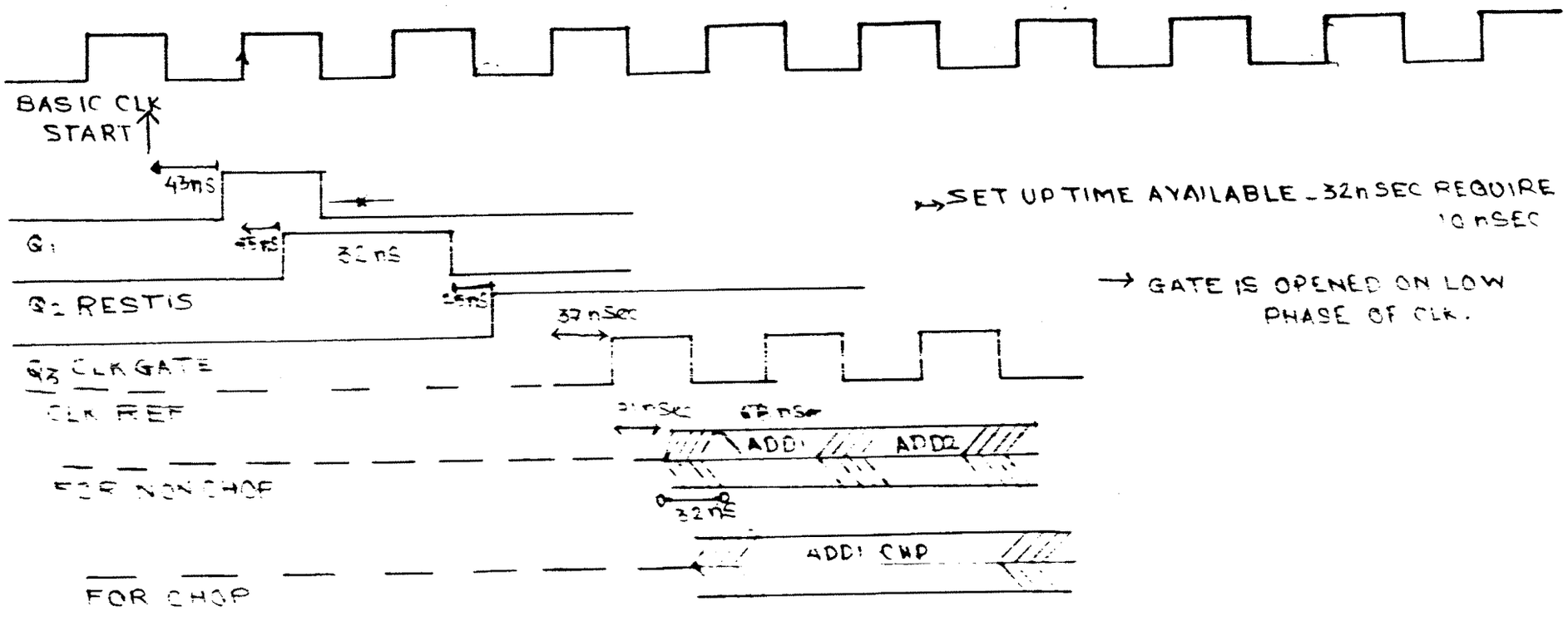


Fig.NO. 3.31a· SLOW MODE ADDRESS GENERATOR·



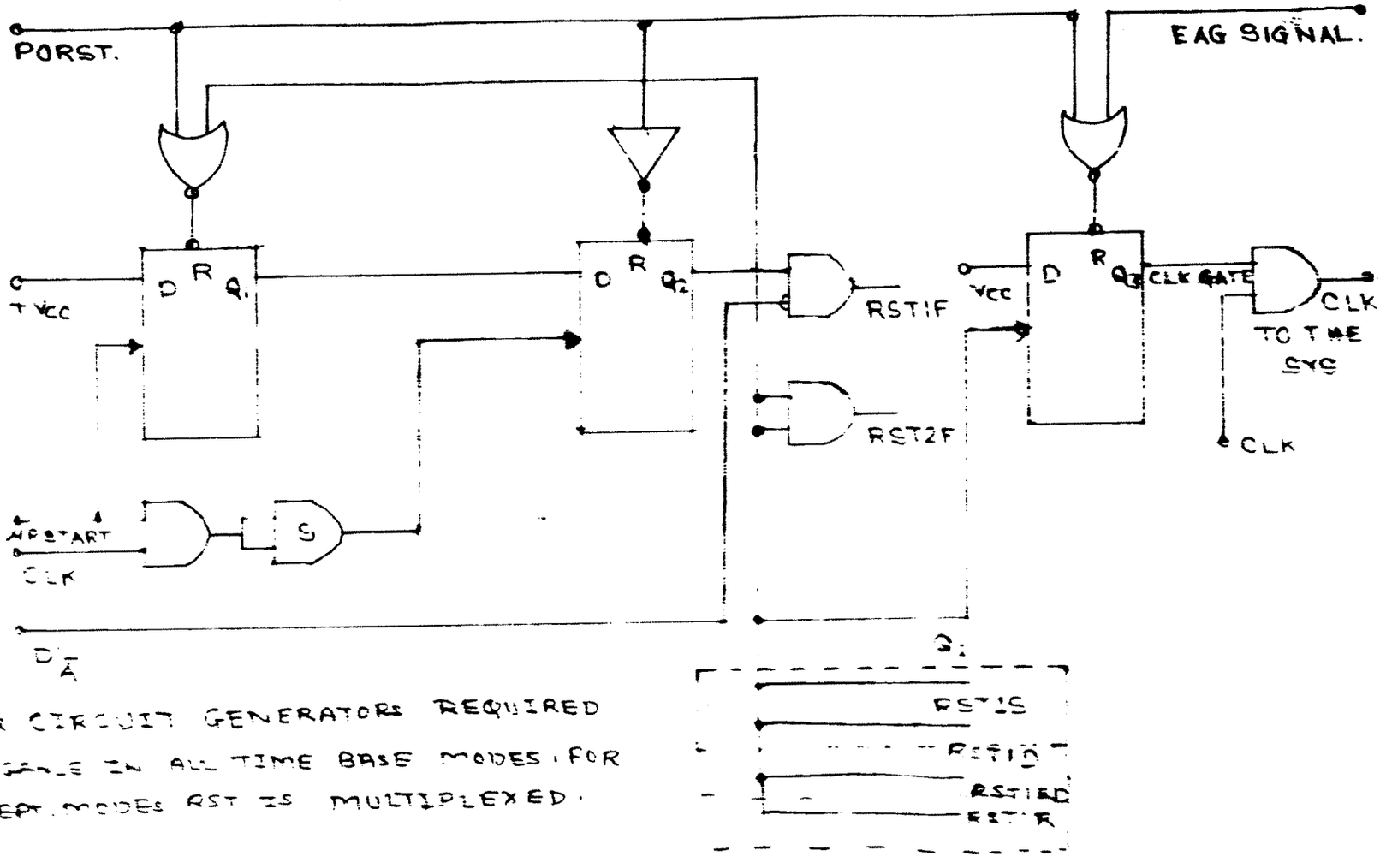
NOTE:- FOR UN TRRIGGER - START OCCORES FOR UP START
FOR TRIGGER START EVENT OCCORES FOR UP START + TRIGGER.
OTHERWISE TIMING ARE SAME
THE DELAY IN THE CLK'S TO DMA AND COUNT ARE MANAGED SUCH THAT IT IS FED AT SAME INSTANT.

Fig. NO. 3-31b SLOW MODE ADDRESS GENERATOR TIMING

The address generation scheme is different in four allowed modes of action (Table 3.21). For all these modes a bi-flip-flop circuit generates a reset signal, after the up has loaded a start bit. In untriggered mode the up start itself causes reset to go active on rising edge of the MSMV clock. The chop mode is always a triggered mode. On the falling edge of RSTIS the clock gate is opened (Fig. 3.31b). The address generator clock is a divided by two clock in the chop mode, the output of the MSMV clock gated with the clock-gate is fed to the ADC clock multiplexer. Each clock line has a specific delay introduced on it, which manages synchronization of acquisition and storage.

In the triggered mode the 11th bit of address generator acts as an end of acquisition/display event [EAG], while in untriggered mode the end acquisition/display is only upon external interrupt. In the save mode the interrupt is generated from DMA address generator. The clock and reset signals for the DMA address generator, active in save or save display modes, is also generated within this block. The DMA operation is also in the count up fashion.

2) Fast Mode Address Generator : The address generation facility in this mode is a lot elaborate. Two reset signals are required for this activity, the RST1F appears only in the beginning of the acquisition event, while RST2F appears for both the acquisition and the display events. The circuit meant for generation of RST1F, RST2F and clock-gate are similar to those discussed for slow mode. Therefore the circuit only is given in Fig. 3.32, but the



1) SIMILAR CIRCUIT GENERATORS REQUIRED FOR RESET SIGNALS IN ALL TIME BASE MODES. FOR FAST & REPT. MODES RST IS MULTIPLEXED.

Fig NO 3.2 SYNCRONEOUS RESET GENERATOR.

explanation is anticipated.

The µp interface initially loads the pretrigger count, if it is supplied, otherwise it is treated as zero. Two 10 bit counters are used in parallel in this mode, Fig. 3.33a. The lower and upper counter banks, accumulate the memory address count simultaneously. The count in the lower counter is subtracted with the pretrigger count set [addition with first compliment]. Further, if a trigger appears after the count accumulated in a lower counter is greater than pretrigger count, then the lower counter is disabled from counting. A subtractor is used between count accumulated in lower counter and the pretrigger count. The subtracted count and the upper address counter are compared such that acquisition of 1K only will appear, positioning the trigger properly. The subtractor [A > B] generates an interrupt to processor indicating end acquisition and simultaneously disables the clock-gate.

In a situation where trigger is not received in 1K acquisition, a flip-flop is set to indicate 'No trigger' received, and disables the clock-gate. In this case another interrupt is generated to indicate no input signal. Various features of timing are shown in the Fig. 3.33b, 3.33c, 3.33d.

In the save and save display mode RST1F is disabled. Counter acts as an up counter and the interrupt is generated from the DMA address generator.

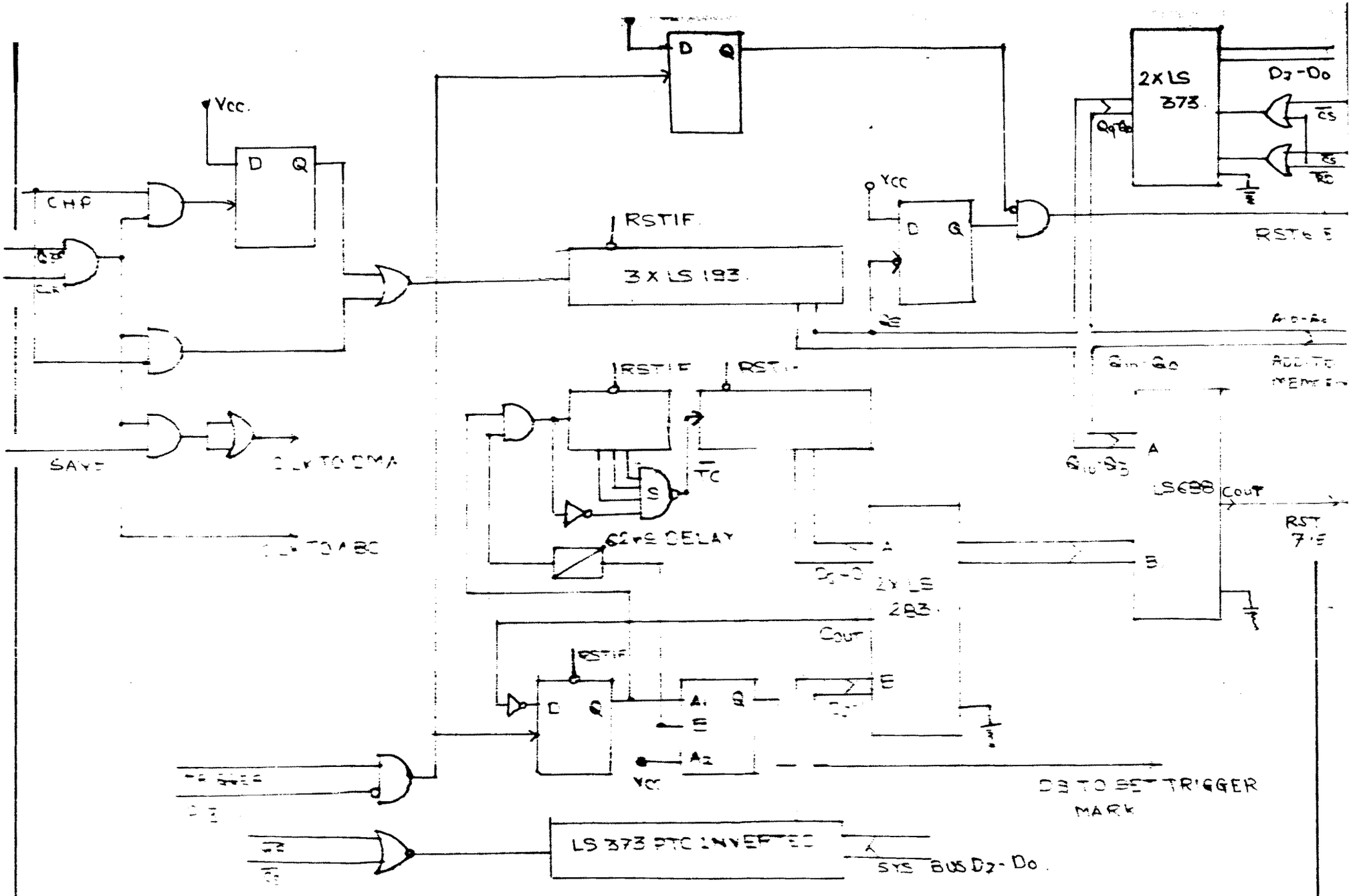


Fig. NO.3-33a FAST MODE ADDRESS GENERERATOR

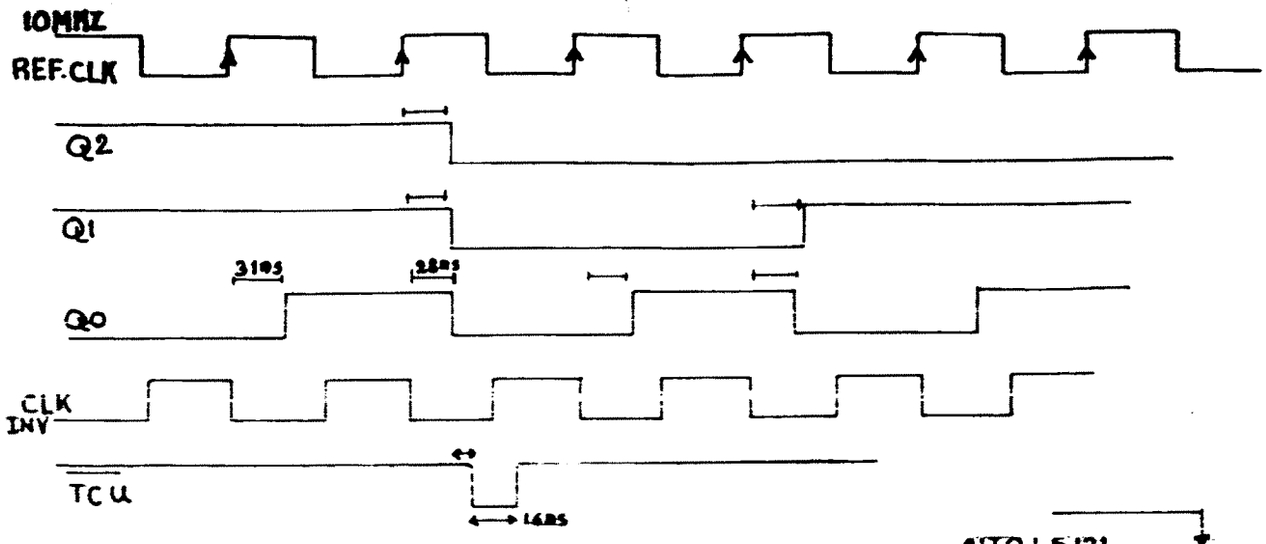


Fig. NO. 3.33 b. SECONDARY COUNTER ALTERNATE $\overline{TCU}$ TIMING

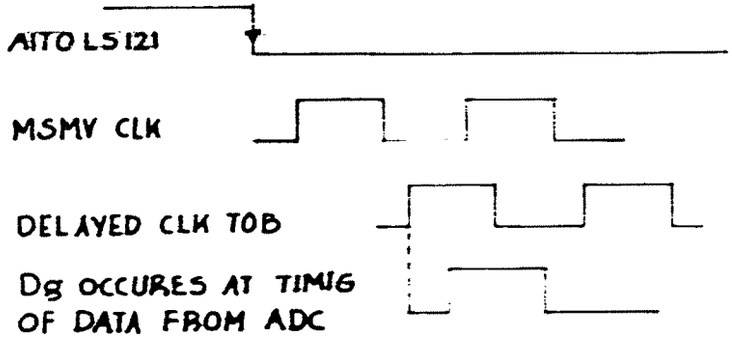


Fig. NO. 3.33c TRIGGER MARK TIMING

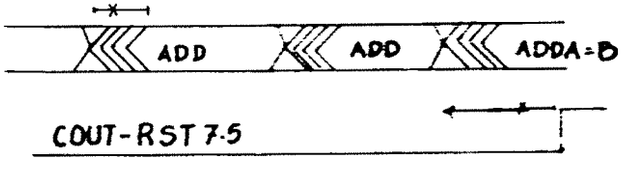


Fig. NO. 3.33d RST 7.5 DELAY TIMING

3) **Repeatative Mode Address Generator** : This circuit is explained by dividing it into three blocks.

i) The vernier counter : It is meant to count time gap between the rising edge of acquisition clock and the trigger. The philosophy of start, reset and the clock-gate are the same except that proper TTL to ECL conversion is necessary. The basic unit is a modified version of vernier counter (34) operating at 50MHz main clock and the vernier clock is at 62.5MHz. Further the symetric 50MHz and 62.5MHz clocks, generated using ECL OR & NOR gates are subjected to monostable multivibrator circuit. The resulting clock is with - 3nsec pulse width and the clock generators could be activated externally. The clock output will be low in the deactivated state of the clock. Upon activation, the first rising edge will appear out of the clock circuit. The delays encountered are shown in Fig. 3.34b. The clock durations of 50MHz and 62.5MHz are 20nsec and 16nsec respectively, Therefore the correspondance will appear for vernier count of less than 5.

The vernier counter proposed accepts trigger after the clock-gate is activated, the maximum time difference to be counted is 100nsec because the clock frequency at 10MHz for the repeatative mode. The following discussion relates to the estimation of the least count.

The time base range covered in repeatative mode operate at time base settings of 5 μs/div, 2 μs/div, 1 μs/div, 0.5 μs/div. Table 3.31 gives the number of acquisitions for each horizontal scan and a statistical estimate of number of repeatation [slot

weight] required to acquire the 1K samples. For the time base settings of 0.5 μs/div within each horizontal scan 20 samples are acquired and therefore minimum measurable time between a trigger and a positive edge of acquisition clock becomes 4nsec. With the scheme of the vernier counter proposed the least count reduces to 2nsec.

Table 3.31

For Repeatative Mode Operation

Timebase setting	No. of Acq. required	Slot Weight	No. of samples/ acq. cycle
5 μs/div	5	5	200
2 μs/div	5	5	200
1 μs/div	10	10	100
0.5 μs/div	20	20	200

The control circuit unables the 50MHz counter upon trigger and the counts are accumulated in main counter till next positive edge of acquisition clock. Upon positive edge of the clock the vernier clock generator is activated and counting proceeds in the vernier counter. Instead of an AND type of correspondance detector, a OR and flip-flop combination is used. The delays encountered in the correspondance circuit are such that the counter module proposed does not remain error prone, though the main counting is displayed right on the positive edge of acquisition clock (For the details please refer the Fig. 3.34a and timing diagram Fig. 3.34b). The count in the main and vernier

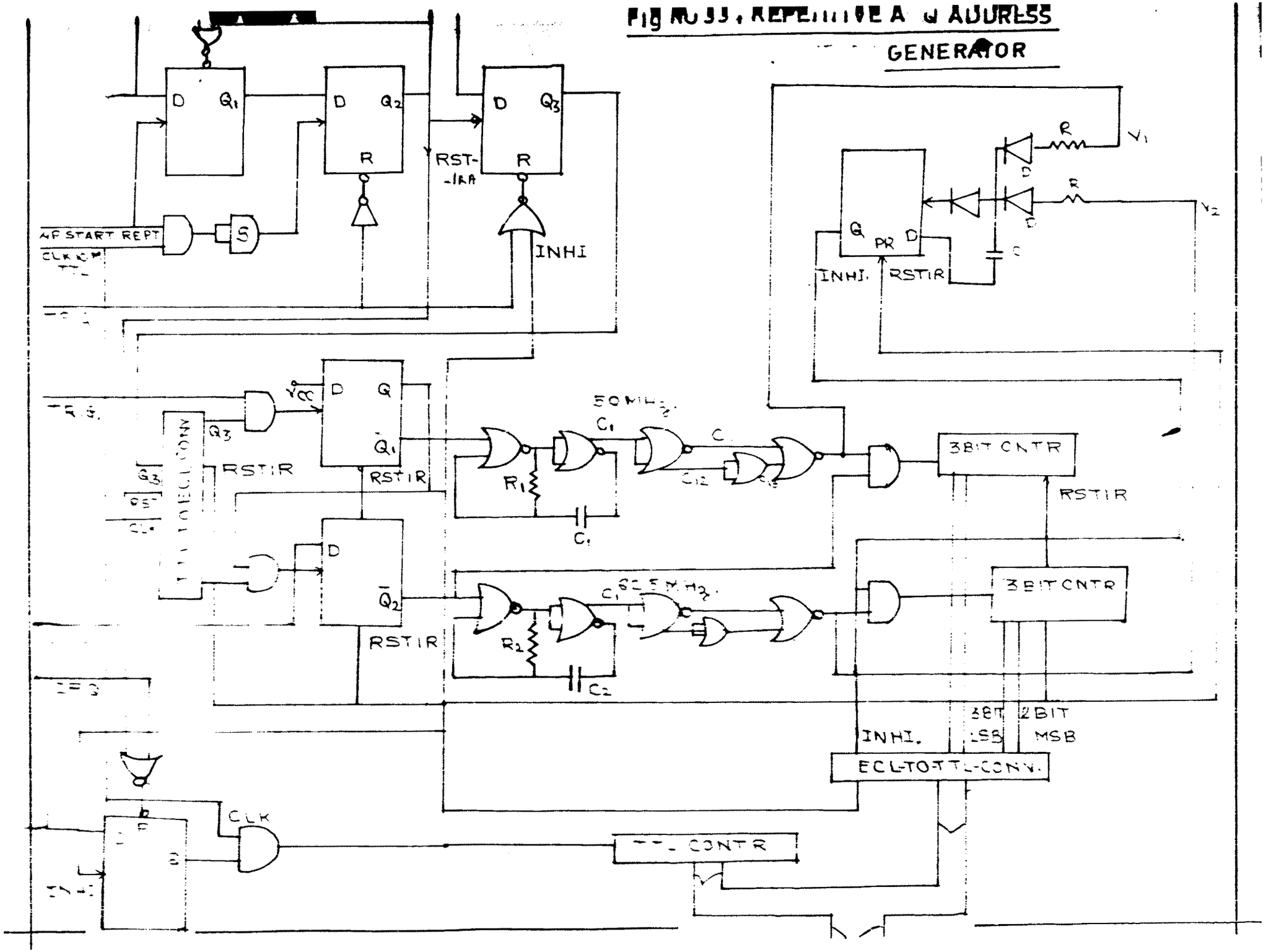


Fig No 33, REPETITIVE & ADDRESS

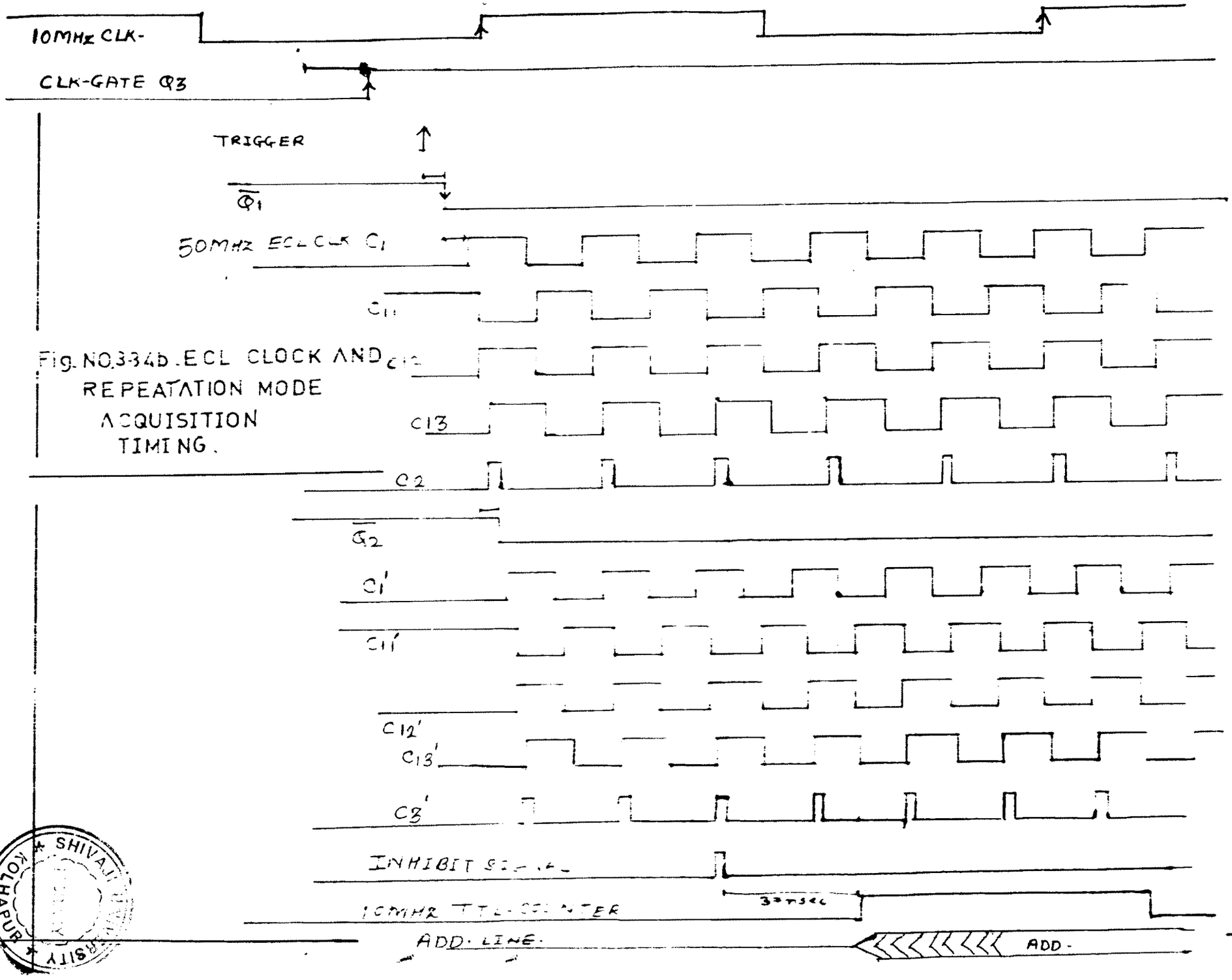


Fig. NO.3-34b. ECL CLOCK AND REPEATATION MODE ACQUISITION TIMING.

NOTE:— SIMILAR TYPE OF LAYING IS FOR ADD. LINES,

THE SLOT SELECTION IS FROM up; CONNECTED TO THE BUFFERS; GIVING RISE TO ADDRESS MULTIPLEXIG.

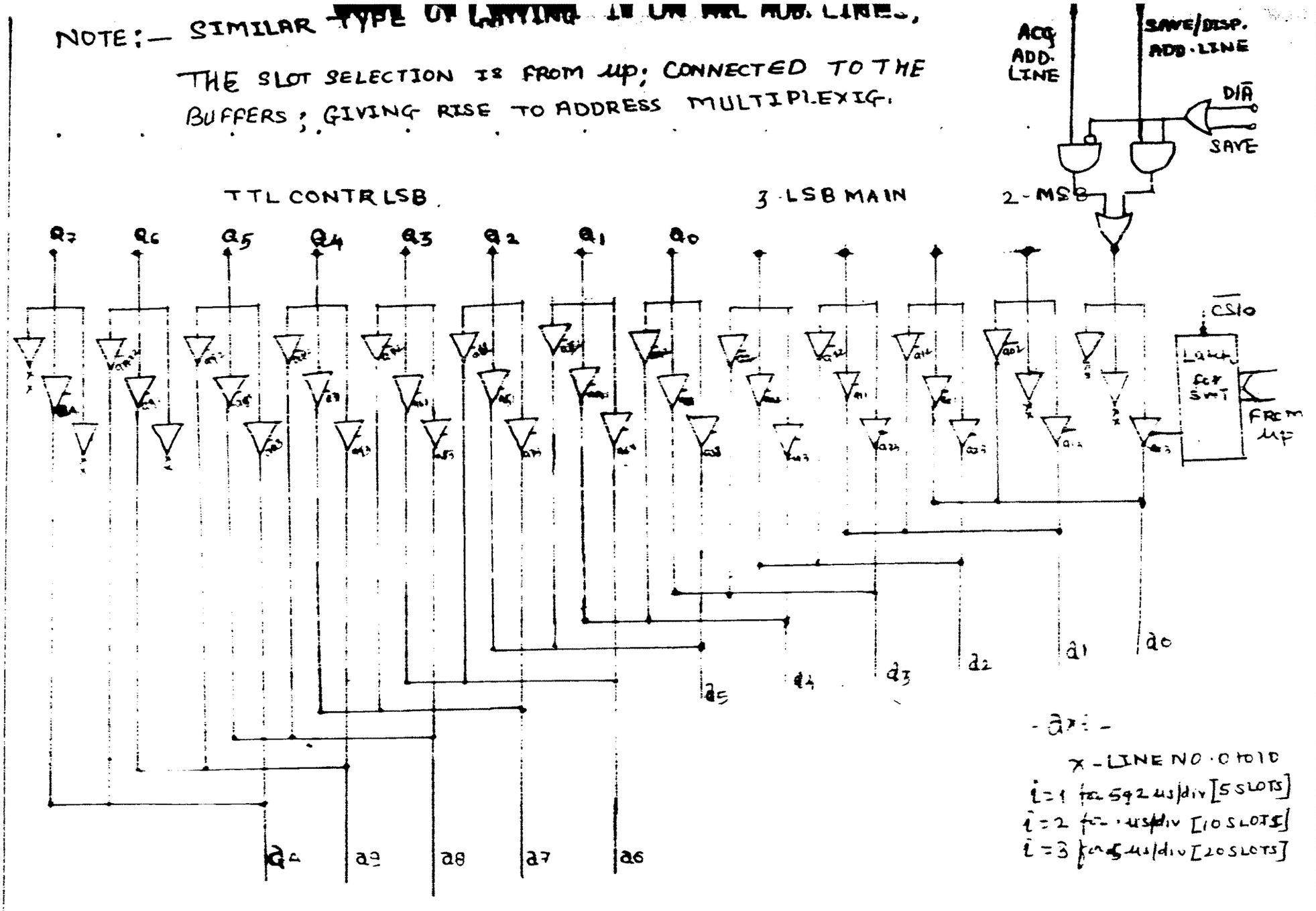


Fig. NO. 334c ADDRESS MULTIPLEXING WITH SLOT

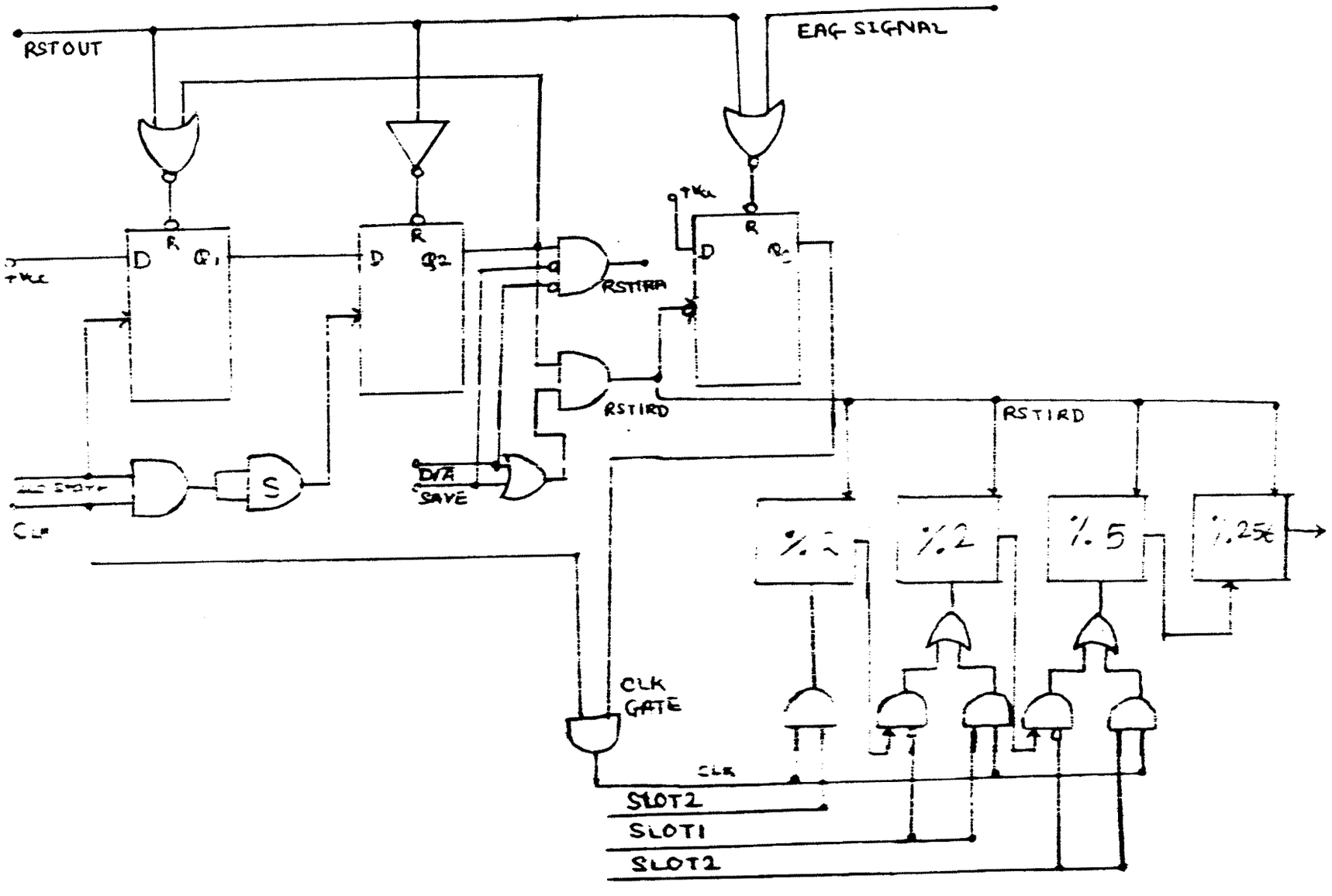


Fig. NO. 334 REPT. DISPLAY MODE ADDRESS GENERATOR

counter provides the slot to be acquised.

ii) Memory address generator : The inhibit signal from the corresponance circuit openes the clock-gate for the secondary counter, a TTL device. The TTL counter is managed to be of 8, 7 and 6 bits effectively. (Fig. 3.34a)

The slot word generated within ECL vernier counter is properly ECL to TTL converted. Dependent on the time base settings either three or four or five bits of vernier counter are used to indicate the slot. The slot bits and the secondary counter form the 11 bit memory address. Because of the difference in counts of decimal and binary counting systems 5 out of 8, 10 out of 16, or 20 out of 32 memory location are acquised or retrieved for time base settings 5 μs/div & 2 μs/div, 1 μs/div or 0.5 μs/div respectively. Therefore within a block of 1.6K of acquisition memory the 1K samples are systematically distributed. The next bit to the MSB of secondary counter provides end acquisition signal [EAG]. The Fig. 3.34c shows multiplexing of the address lines dependent on time base settings.

iii) Display address generator : While displaying the acquisition data in the repeatative mode, the systematisation at the acquisition time is to reproduced in counting. Therefore the address counter Fig. 3.34d is a multiplexed version, where it acts as either (a) divided by 5, divided by 256, (b) divided by 10, divided by 128, (c) divided by 20, divided by 64 counter. Dependent upon the time base settings, one of these mode is selected. The counting procedure in mode (a), mode (b), or mode

(c) for 5, 10 or 20 slotted acquisition/display scheme respectively (Table 3.21). (The data sheets of components in the vernier circuit are reproduced in Appendix).

4) Display Read-out Circuit : The philosophy of start and clock-gate is similar in this mode of operation also. The basic 20MHz clock is divided by 8 and used as the system clock for this circuit, Fig. 3.37. The X-deflection is controlled by a 10 bit counter, output of these counters are subjected to D/A conversion and fed to the X final amplifier, after proper conditioning and multiplexing (Fig. 3.35).

The Y-position is controlled through a 8 bit latch/counter operating in the up mode. Within a display interval, only 3LSBs of the counter are modified. Y-position is fed to the Ch1 final amplifier Fig. 3.35. The clock for Y-deflection is a divided by 1024 clock. The up loads the count E0 in the Y-counter and is incremented after each horizontal scan up to E8 and the process is repeate.

A [32 X 8] RAM is used to store the display charactors. In the display mode of circuit these charactors form address of a TTL character generator ROM in combination with the Y-address. The character generator outputs the illumination control byte to a shift register corresponding to each character. The data loaded parallely in to the shift register is shifted to Z control of the scope. Each character has 8 illumination bits therefore a 5 bit counter operating at 1/32nd of the system clock is used to

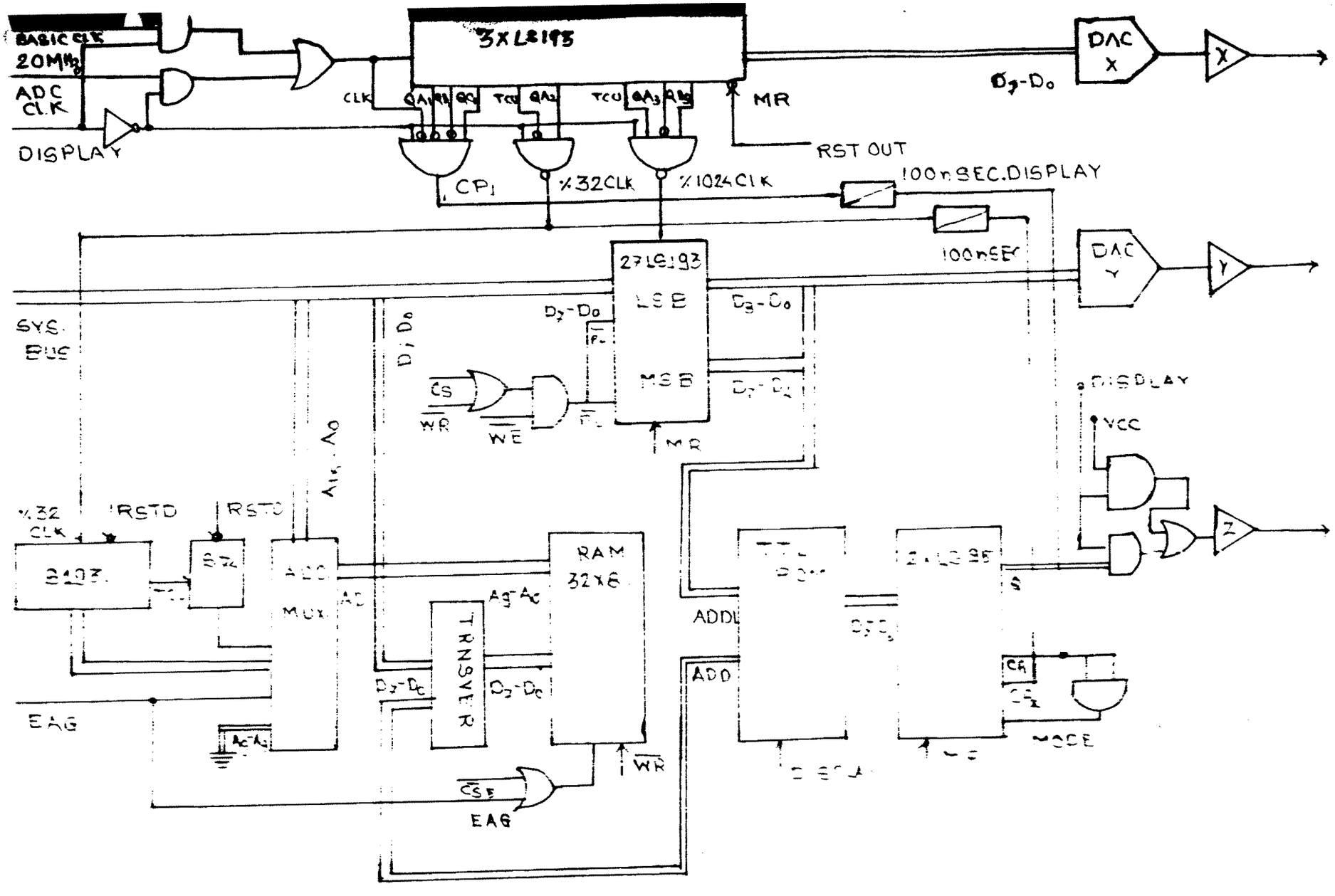


Fig NO335 DISPLAY CIRCUIT

generate the display character address.

Display of information and the signal is achieved through the same circuit. The multiplexing occurs at the level of display mode selection. A few points to be noticed are as below.
a) 1/n clock deviced are of $\overline{TCU}/\overline{TCD}$ type. b) Parallel loading of information into the shift register at 1/32 and serial output at 1/4 clock rates, occur on LSB transitions X 11 to X 100 and X 100 to X 101 respectively. Therefore no event clash is predicted.

5) Memory Components and Configurations : The acquisition memory is a 4K X 9 configuration for the DSO circuits. On the other hand the same configuration appears splited as a sets of 4KX8 and 4KX1 [8] configuration for the up interface. The address of this 8K block are mapped continuously. The memory componants proposed are NMC2148-3/NMC2148L [4K X 8] and MM2147-3 [4K X 1], with read/write cycle timing of 55nsec. 2 X 2148-3 form a 1K X 8 unit, two such units are combined to form data acquisition memory, referred as MCh1 and MCh2 (Fig. 3.36). The data sheets of the memory component are reproduced in Appendix.

A 4K X 8 memory unit, selectable as a 1K page at each time, is used to store [Save] the acquised and properly trigger centred information. The information stored is always of one screen width and therefore block of 1K X 8 is necessary and sufficient. The appropriate block is selected through the software. [Fig. 3.37]

Refering to the timing diagrams in, Figs. 3.31b, 3.33b, 3.34b it is apparent that the address is stable on the address bus

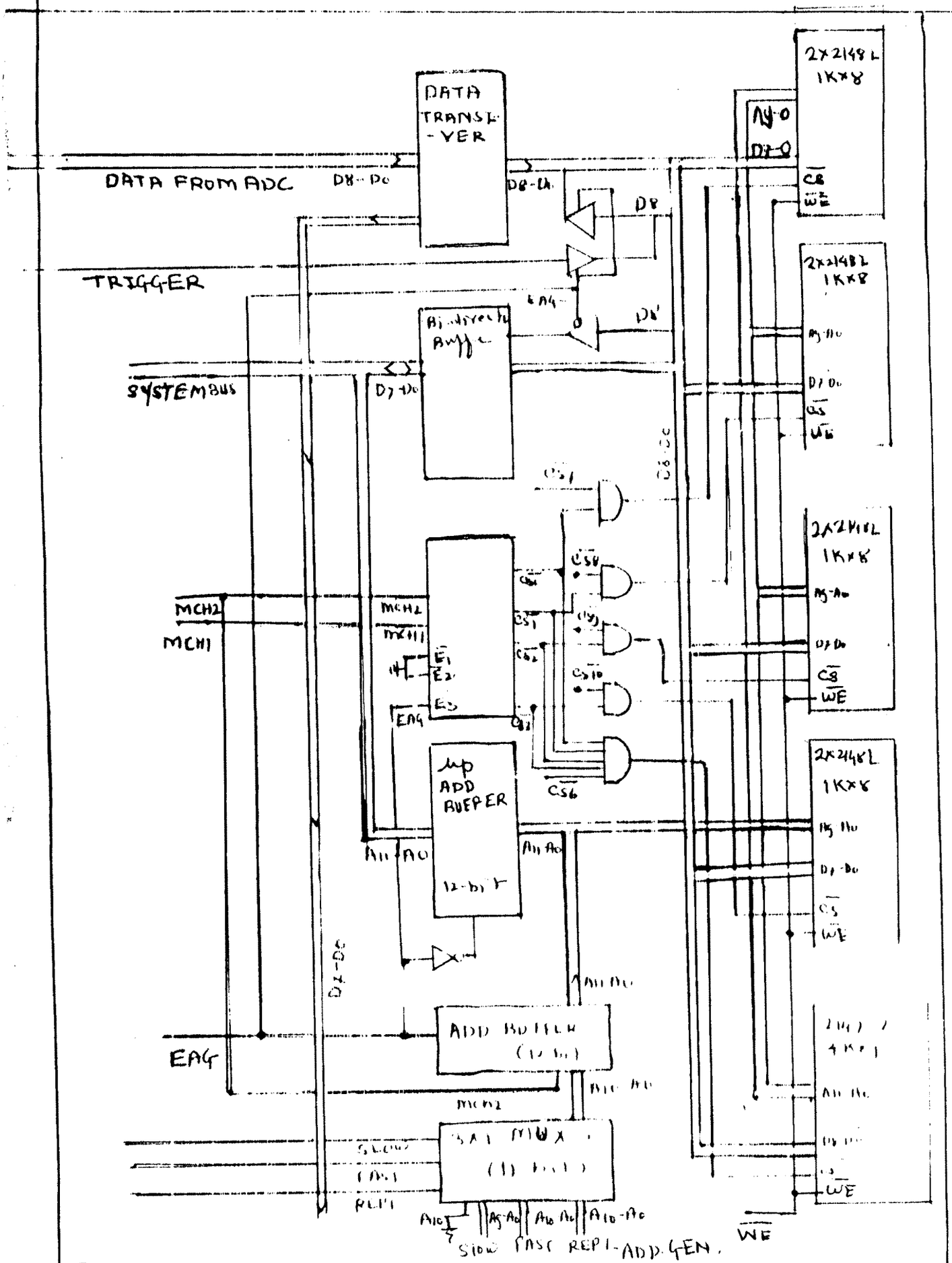


Fig. NO.3-36 ACQ. MEMORY CONTROL CIRCUIT

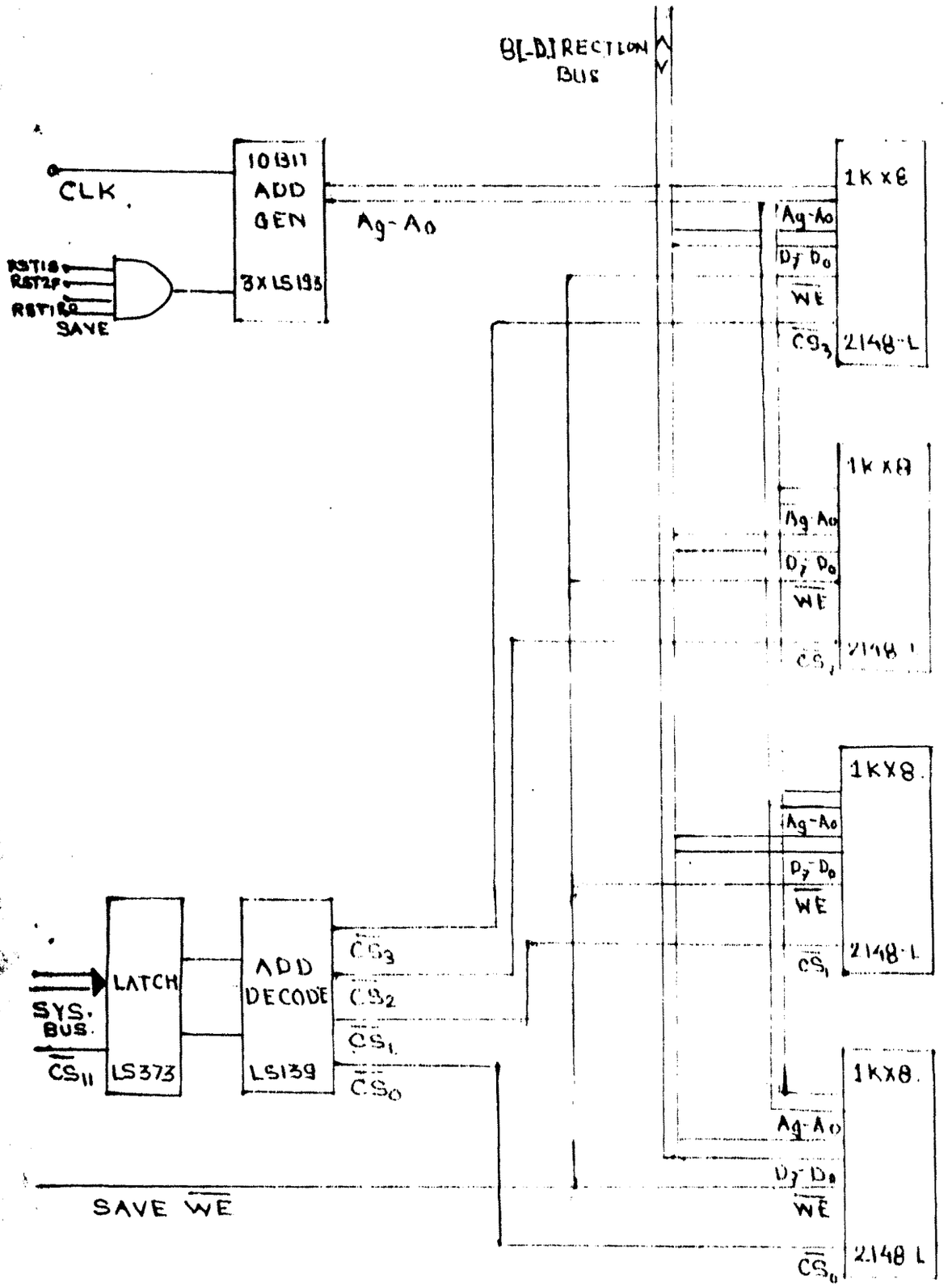


Fig. NO. 3.17. DMA AND MEMORY CIRCUIT

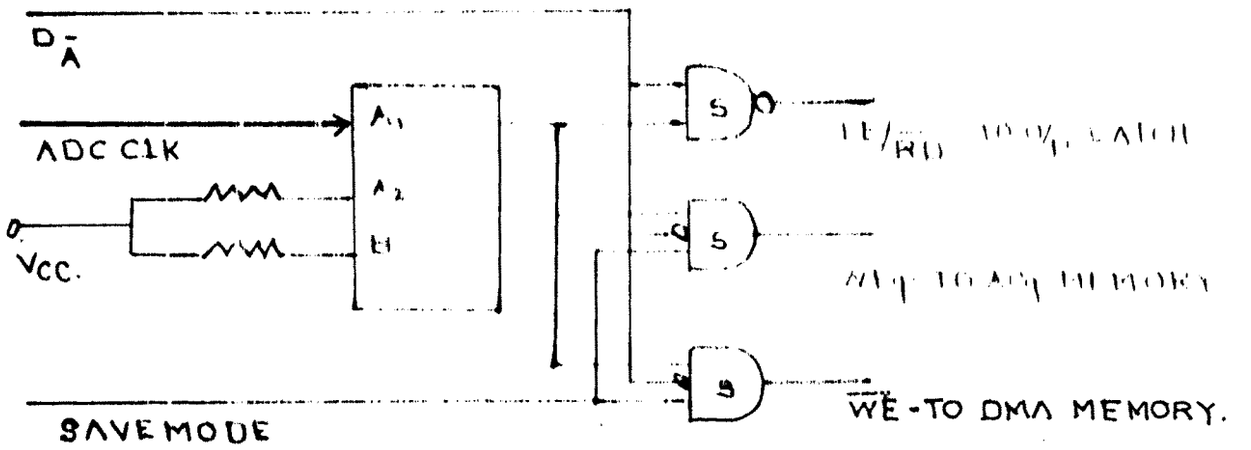
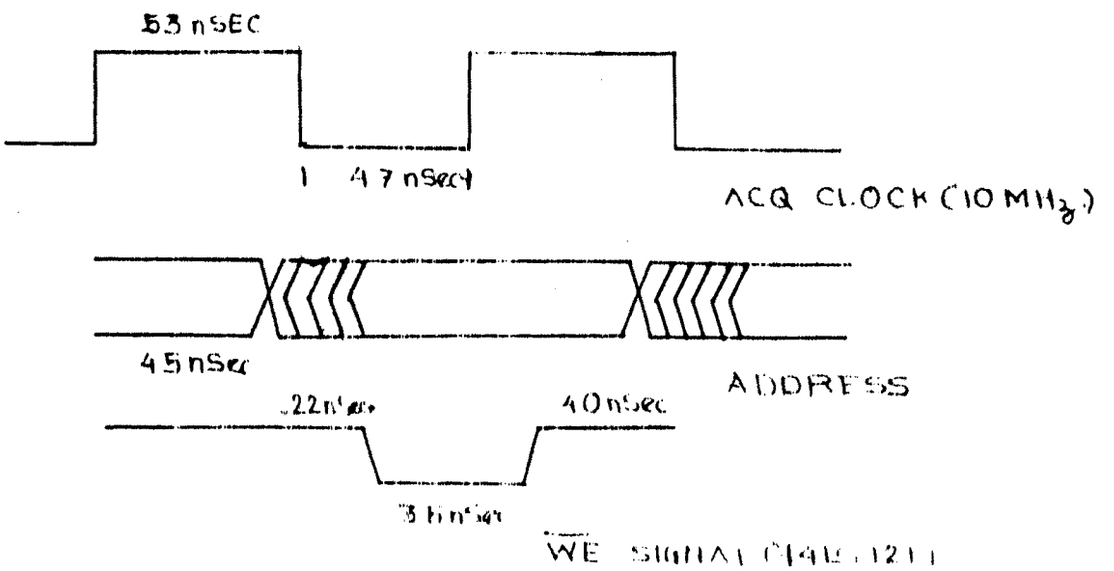


Fig. NO 3·38a CONTROL CIRCUIT FOR WE.



NOTE:- TRIGGER IS ON ↓ OF A, THE A TO Q DELAY AND PULSE WIDTH WILL BE ADJUSTED WITH VARIOUS C_1 CONTROL

Fig. NO. 3·38b CONTROL CIRCUIT FOR $\overline{WE}$ TIMING.

at a time instance, which is 42nsec apart from the acquisition clock pulse. Further referring to the timing diagram (Appendix). of the ADC 3308, the digital o/p is available after about 20nsec from the end of acquisition phase. Reconciling with these timing features and paying an attention to the memory requirements, a $\overline{WE}$ control generation/multiplexing circuit is designd The circuit employs a monlithic monostable multivibrator 74LS121. At present the device is proposed to operate without external timing capacitor and generates a monostable pulse of approximately 35nsec (These features are elaborated in Sec. 3.1). These features satisfy the timing requirements of the configuration proposed.

Various tri-state devices proposed to transive the address and data bus of the memory configuration, is a too standard and a prototype configuration. The various chips proposed for the purpose are [74LS244, 74LS245]. To avoid reproduction of the standard design data (36), the details are assumed.

Regarding the additional hardware overhead of address generation for the DMA cycles, the circuit and the memory configuration is given in Fig. 3.38a, 3.38b, clock to this address generator appears from one of the address generators selected according to the time base setting. Reset caused before the operation starts, resets the counter. In saved data operation mode, both the address generator run simultaneously in the count up mode. The terminal count of the address generator is used as an interrupt signal, in the display mode, though the clock is fed to the DMA circuit, the address generation for the acquisition memory

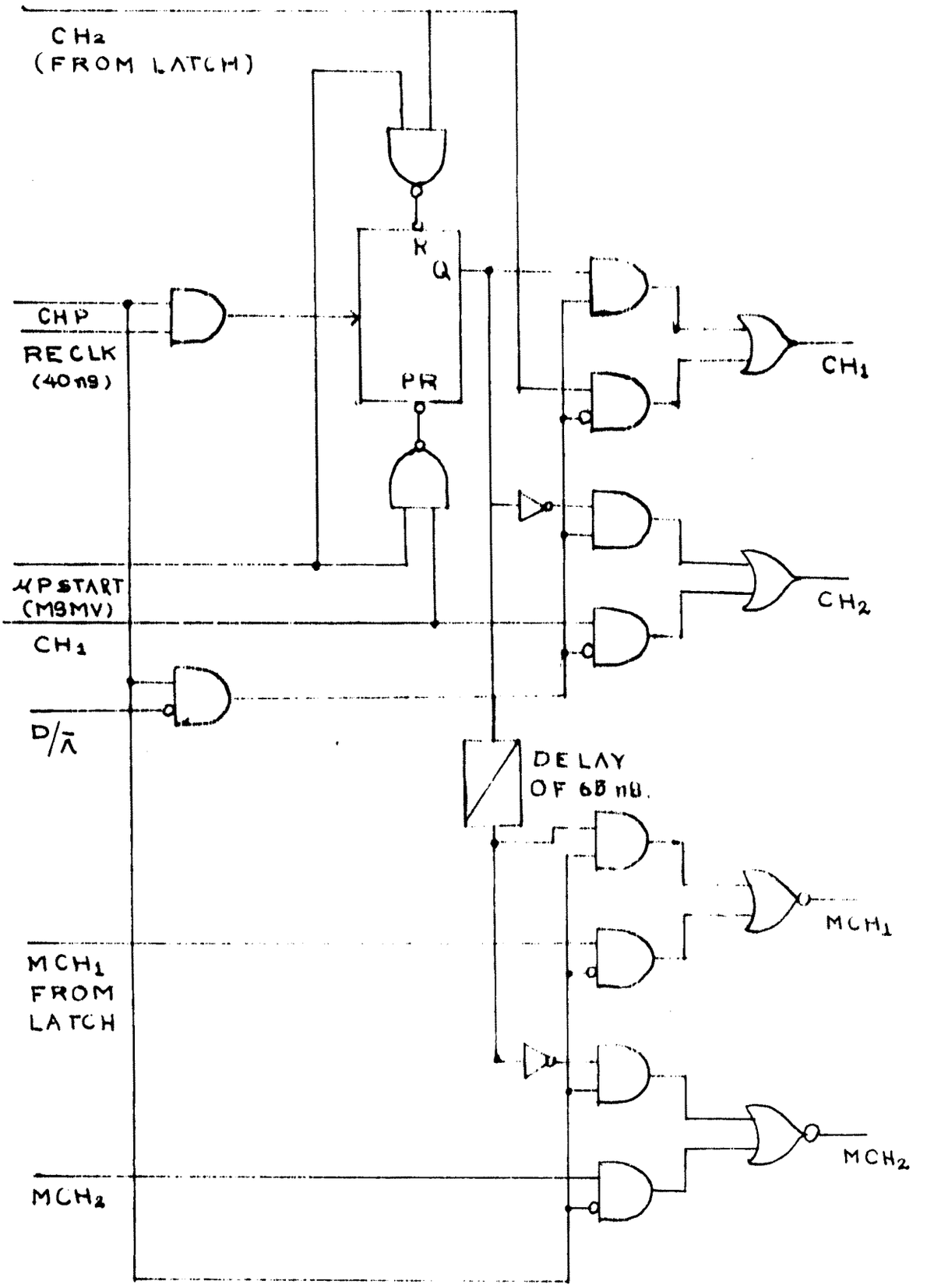


Fig. NO. 3.39 CHANNAL SELECT LOGIC.

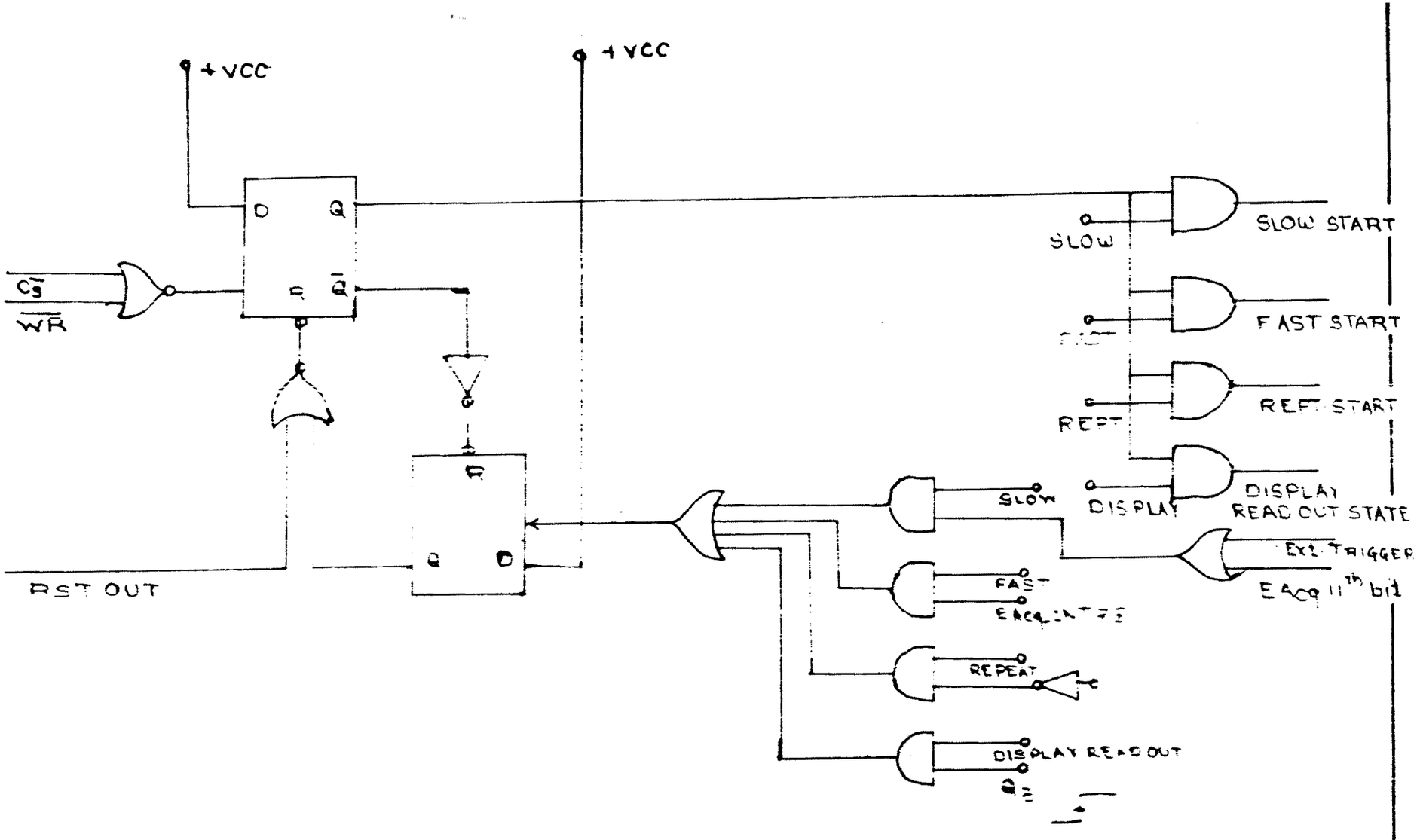


Fig. NO. 3.39 µP START MULTIPLEXING.

is withheld.

6) Other Multiplex Controls : The Table 3.21 accounts for the control signals required to execute a desired operation. μp is meant to latch these control signals as per requirement. These control signals could be grouped in to two sections (a) Initialisation controls and (b) Mode selection controls. The initialisation controls are meant basically to select one of the address generator and related control and multiplexing. This is achieved through a resetable latch 8212 [Reseted after each power on activity]. If the 8212 is reseted the information display mode is selected automatically. The remaining modes are selected through software.

The mode selection control - this group of signals include Ch1, Ch2, MCh1, MCh2, D/$\overline{A}$, Chp .... etc. (Table 3.21 provides the meaning of these signals). μp is exclusively meant to select a mode of operation and therefore to set the proper mode control word. [Fig. 3.39]

7) Clock Generator : The span of clock frequencies required for the standard 20MHz oscilloscope lies between the range 500Hz to 10MHz. The calculation assumes 100 acquisition/div and the maximum data conversion frequency of 10MHz. Despite of the actual values the range becomes an important factor while designing a timer/clock generator. The basic clock is generated using monolithic IC 424 and is of 20MHz. Secondly the on time required of the output clock is of 50nsec only. A 15 bit counter operating in the count down mode is used for the purpose. The counter is

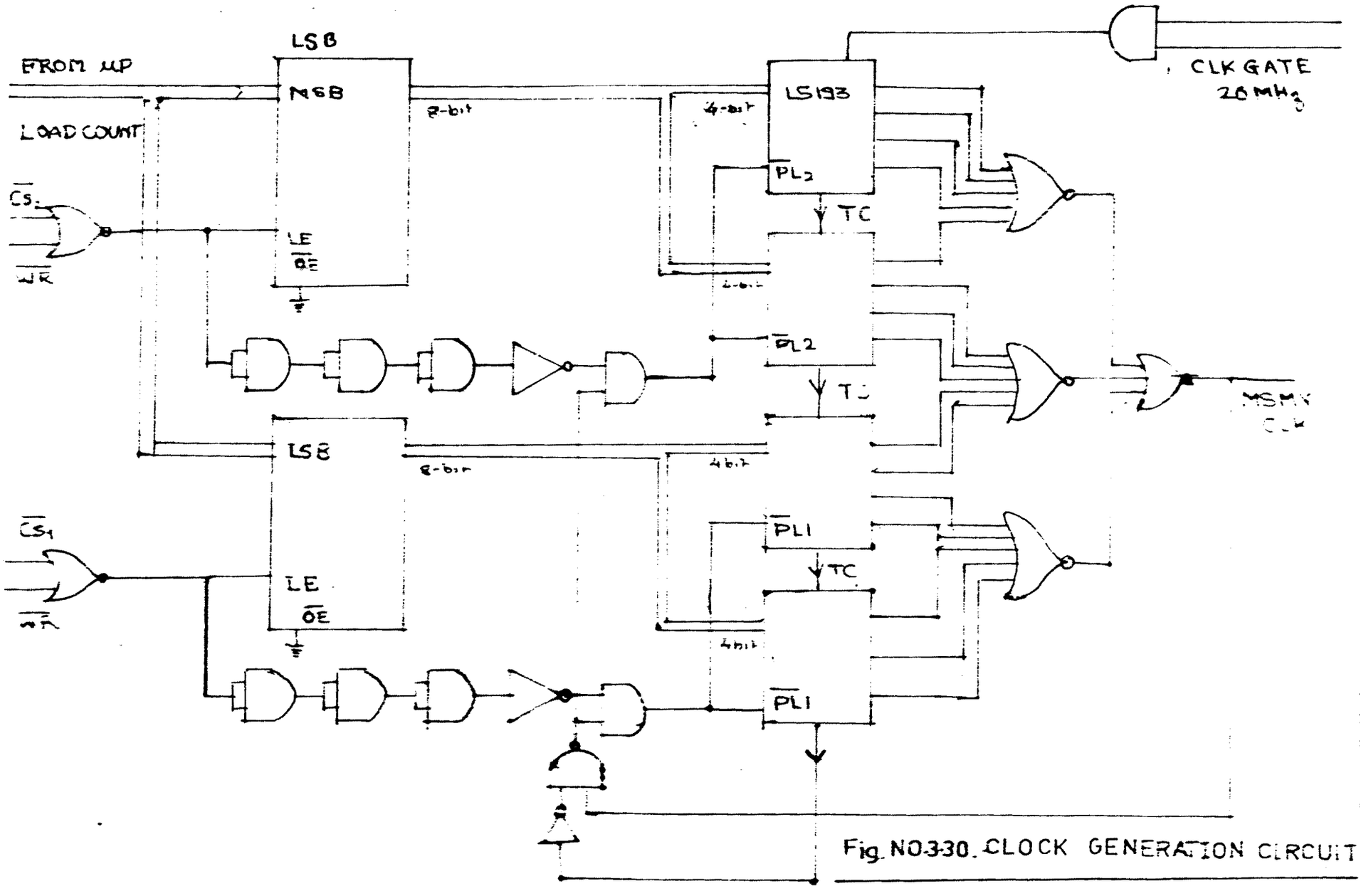


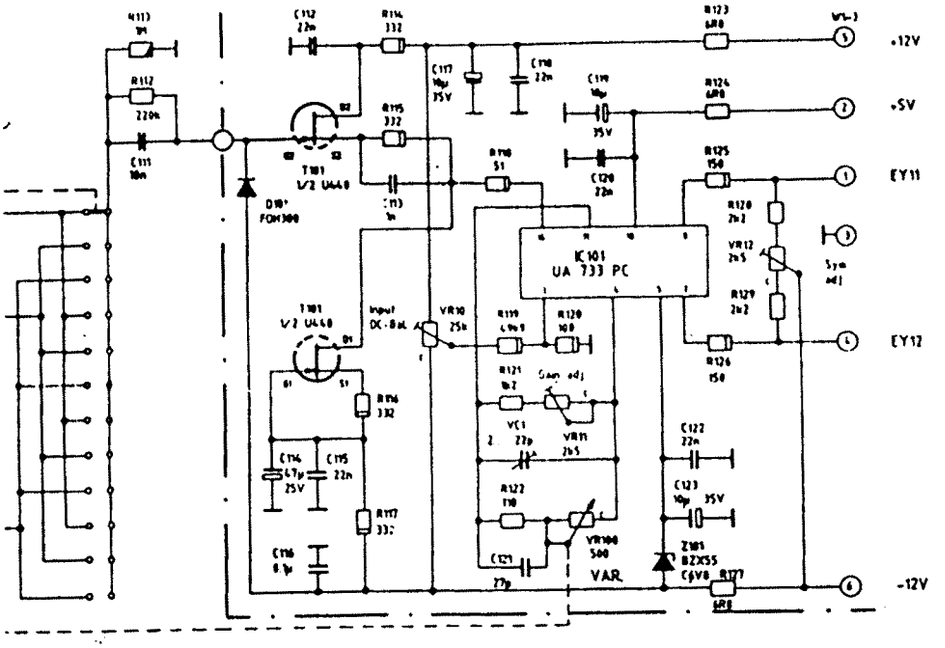
Fig. NO 3.30. CLOCK GENERATION CIRCUIT

initially loaded from a up addressable latch and by up itself. Upon each count down the counter is reloaded automatically from these latches. A XNOR circuit, operating on 15 bits of count down word, generates a monostable pulse. The output is high for the terminal count [$\overline{Tc}$] only. The circuit diagram is given in Fig 3.30.

3.4. THE ANALOG INTERFACE HARDWARE :

The preamplifier used in HM 203 is a FET input amplifier with IC μA 733 as amplifying device. The circuit is powered symmetrically with $\pm$ 5V supply. The rated range of output swing is guaranteed to 3 volts symmetric output form μA 733 [a balance symmetric output operational amplifier]. The signal is further subjected for amplification through a switchable stage. The channel selection is realised at this stage. Fig. 3.41 reproduces the relevant part of the circuit diagram of HM 203 and the switchable amplifiers are encircled in the Fig. 3.41. At present we propose to use the similar switching logic to switch the input channels.

After the channel inputs are switched the symmetric output will be converted to a single ended output like that of conventional operational amplifier and the gain of the circuit will be so adjusted that the output swing occurs between 0 to +6.4 volts maximum. The switching circuit being principally the same, it has not been subjected for performance test. The design data of 3308 reproduced in Appendix, shows recommended circuit connection to achieve A/D conversion, where the range of input is



Y-Input, Attenuator, Preamplifier Channel I and Channel II

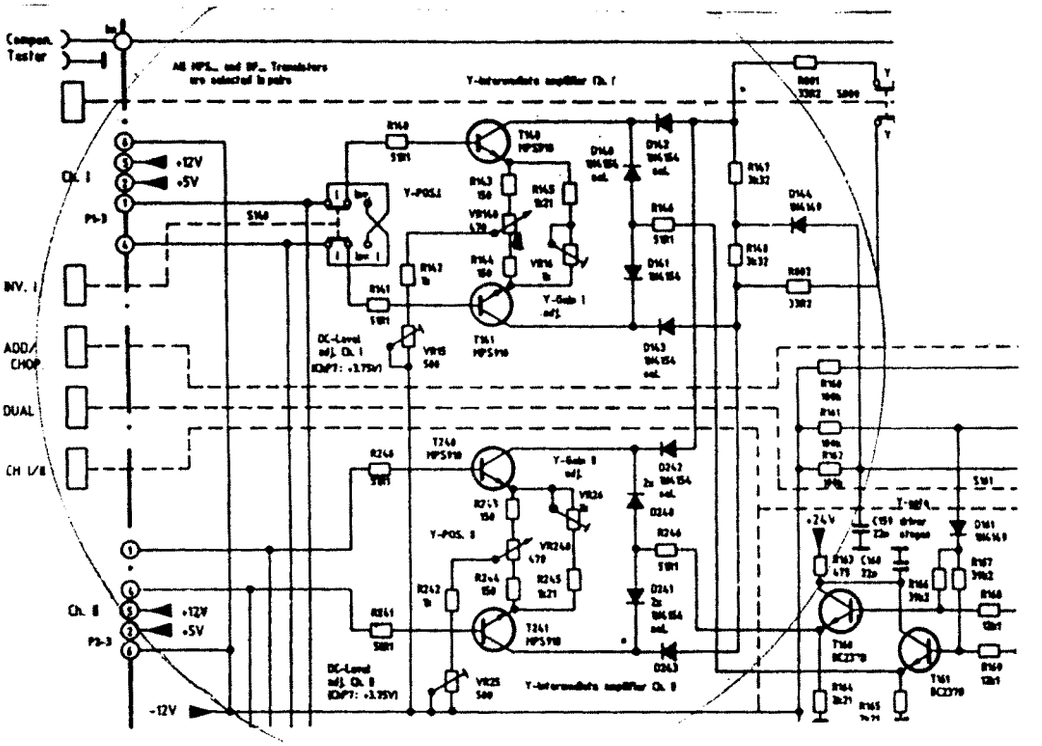


Fig-341 - **Y-Intermediate Amplifier Ch.I u. Ch.II,**

allowed between 0 to 6.4 volts [the level 6.4 volts is desired for the convenience while handling digital quantities].

Digital number 00H will correspond to the voltage level causing deflection to 5 cms below the central line of the CRT, while the quantity FFH will correspond to 5 cms above the central line of the CRT. With DAC 0800, both Io, $\overline{Io}$ output lines are provided (data is reproduced in Appendix). These two could be made use of again to generate a symmetric output, within 3 volts limit. The symmetric output thus generated could be fed to the Y final amplifier with proper input conditioning. The design procedure used for this purpose are taken from the Handbook of Micro circuit Designing Application by Stout and Kaufman (37).

3.5. TESTING OF HARDWARE MODULES :

Continued efforts to procure CA 3308, the flash converter from RCA, in Indian currency, were futile. The enquiries to the authorised dealer * also were repelled with regrate. Therefore we shifted our interest from designing a system with a lesser modes of operation, to a system with increased range of operating modes. For such a system the software requirement is sufficiently complicated. [The software developed is discussed in chapter 4.]

Neverthless, the hardware modules are tested to estimate the performance of individual modules. The performance estimated is at the level of confirmation of the theoretically plotted timing diagrams. The tests are also extended to estimate effects of additional loading capacitor to alter the output delays. At

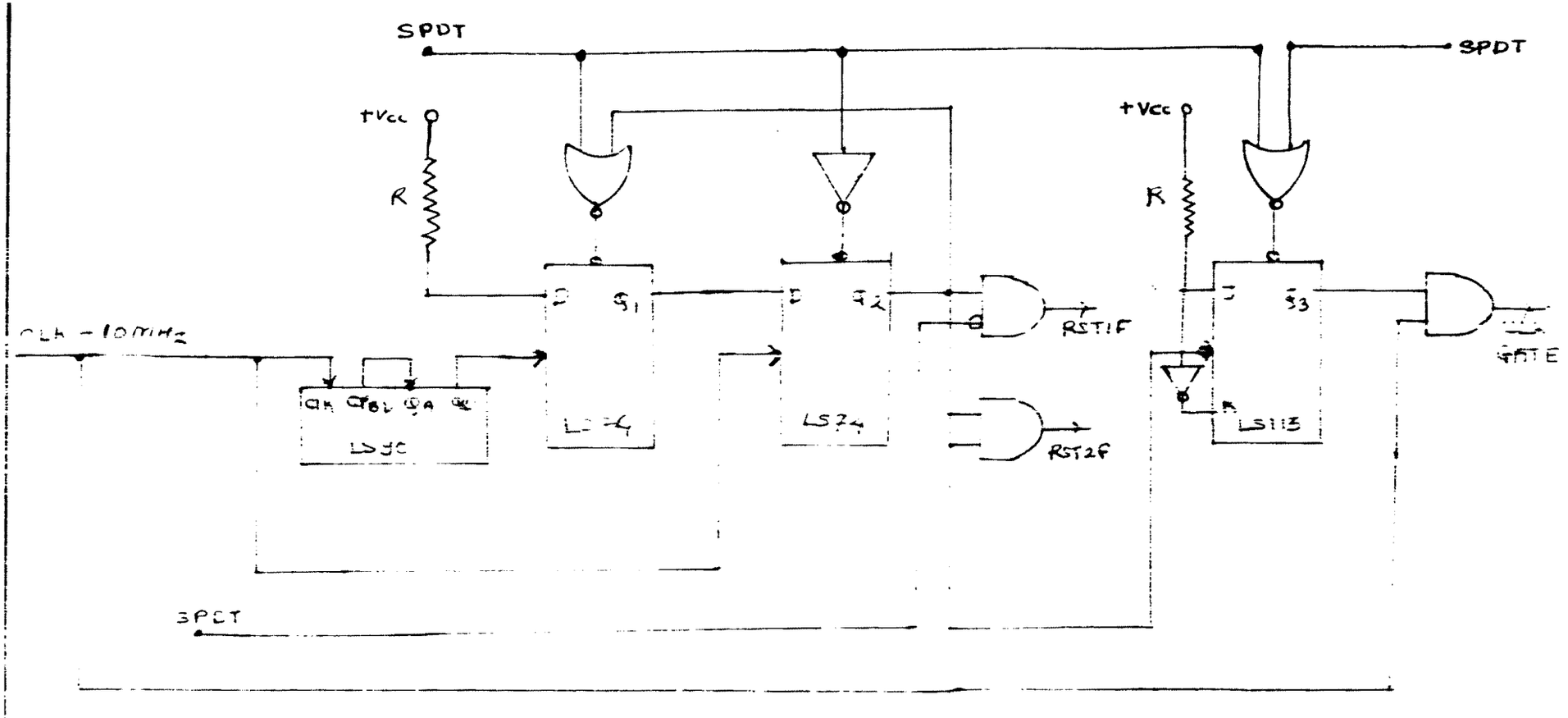
present the department had the 20MHz Pulse/Clock Generator M/s.Scientific Instrument Co. and a 4 CH. - 100 MHz Analog Oscilloscope of HIL5024 and a 100 MHz Digital Storage Oscilloscope from Tektronics. These devices have been fully exploited for the module testing.

The modules tested and its outcome is described below -

i) The bi-flip-flop configuration used to synchronise the operations with the system clock (Fig. 3.32) and a mono-flip-flop circuit getting the clock, appears with each address generator. This circuit has been converted such that it would generate a repetitive signal (Fig. 3.42) to estimate the time delays and synchronisation. The system clock used for this purpose was at 10 MHz. [The maximum clock rate encountered in the DSO interface]. The results are up to the satisfaction and the timing diagrams are confirmed.

ii) The monostable clock generator (Fig. 3.40) employing 2 X LS 193s [divided by 256 max.] was devised and tested. In this case also the clock frequency used is 10 MHz. The observed pulse width was at 110 nsec approximately and with introducing the loading capacitor, could be increase to 115 nsec approximately. The least count of HIL 5024 is 5 nsec/div.

iii) The ECL MSMV clock generator (Fig. 3.34*d*) has also been tested but with the limited bandwidth of the scope the pulse width measurement was not feasible. Therefore instead of a single gate delay two gates were used to generate a pulse of about 10 nsec high time approximately.



NOTE: Up. START GENERATION IS ACHIEVED BY THE COUNTER (LS90)
THE RESET IS DONE BY THE SPDT SWITCH

Fig NO 3.42 SYNCHRONOUS RESET GENERATOR (TESTING CIRCUIT)

The remaining modules are yet to be tested but from the above mentioned test we have gain a confidance in the design and we are optimistic to expect the remaining modules logically correct.