APPENDIX-C

National Semiconductor

DAC0800, DAC0801, DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ± 1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ± 0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ± 4.5V to ± 18V power supply range, power dissipation is only 33 mW with ± 5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

Features

- Fast settling output current — 100 ns
- Full scale error — ± 1 LSB
- Nonlinearity over temperature — ± 0.1%
- Full scale current drift — ± 10 ppm/°C
- High output compliance — −10V to + 18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ± 4.5V to ± 18V
- Low power consumption — 33 mW at ± 5V
- Low cost

Typical Applications

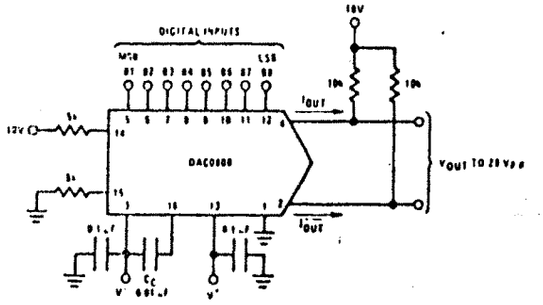
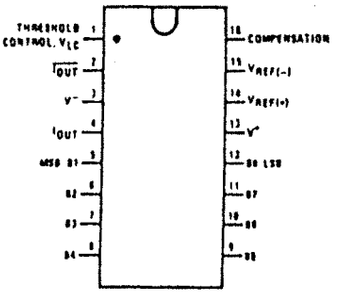


FIGURE 1. ± 20 Vp-p Output Digital-to-Analog Converter

Connection Diagram

Dual-In-Line Package



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See Ordering Information

Ordering Information

Non Linearity	Temperature Range	Order Numbers*			
		J Package (J16A)		N Package (N16A)	
± 0.1% FS	−55°C ≤ T_A ≤ +125°C	DAC0802LJ	DAC-08AQ		
± 0.1% FS	0°C ≤ T_A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP
± 0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LJ	DAC-08Q		
± 0.19% FS	0°C ≤ T_A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP
± 0.39% FS	0°C ≤ T_A ≤ +70°C	DAC0801LCJ	DAC-08CQ	DAC0801LCN	DAC-08CP

*Note. Devices may be ordered by using either order number.

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Absolute Maximum Ratings

Supply Voltage	± 18V or 36V
Power Dissipation (Note 1)	500 mW
Reference Input	
Differential Voltage (V14 to V15)	V⁻ to V⁺
Reference Input	
Common-Mode Range (V14, V15)	V⁻ to V⁺
Reference Input Current	5 mA
Logic Inputs	V⁻ to V⁻ plus 36V
Analog Current Outputs	*Figure 24*
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Temperature (T_A)			
DAC0802L	−55	+125	°C
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0801LC	0	+70	°C
DAC0802LC	0	+70	°C

Electrical Characteristics

(V_S = ±15V, I_{REF} = 2 mA, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter		Conditions	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", T_A = 25°C		100	135					100	150	ns
		DAC0800L					100	135				ns
		DAC0800LC					100	150				ns
tPLH, tPHL	Propagation Delay	T_A = 25°C										
	Each Bit			35	60		35	60		35	60	ns
	All Bits Switched			35	60		35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change < ½ LSB, R_{OUT} > 20 MΩ Typ	−10		18	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R14 = 5.000 kΩ, R15 = 5.000 kΩ, T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	V^- = −5V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V^- = −8V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels											
V_{IL}	Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			2.0			V
	Logic Input Current	V_{LC} = 0V										
I_{IL}	Logic "0"	−10V ≤ V_{IN} ≤ +0.8V		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	2V ≤ V_{IN} ≤ +18V		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V^- = −15V	−10		18	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S = ±15V	−10		13.5	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	*(Figure 24)*	4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS}$	Power Supply Sensitivity	4.5V ≤ V^+ ≤ 18V		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS}$		−4.5V ≤ V^- ≤ 18V, I_{REF} = 1mA		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
	Power Supply Current	V_S = ±5V, I_{REF} = 1 mA										
I^+				2.3	3.8		2.3	3.8		2.3	3.8	mA
I^-				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
		V_S = 5V, −15V, I_{REF} = 2 mA										
I^+				2.4	3.8		2.4	3.8		2.4	3.8	mA
I^-				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
		V_S = ±15V, I_{REF} = 2 mA										
I^+				2.5	3.8		2.5	3.8		2.5	3.8	mA
I^-				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF} = 1 mA		33	48		33	48		33	48	mW
		5V, −15V, I_{REF} = 2 mA		108	136		108	136		108	136	mW
		±15V, I_{REF} = 2 mA		135	174		135	174		135	174	mW

Note 1: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the dual-in-line J package must be derated based on a thermal resistance of 100°C/W, junction to ambient, 175°C/W for the molded dual-in-line N package.

Typical Applications (Continued)

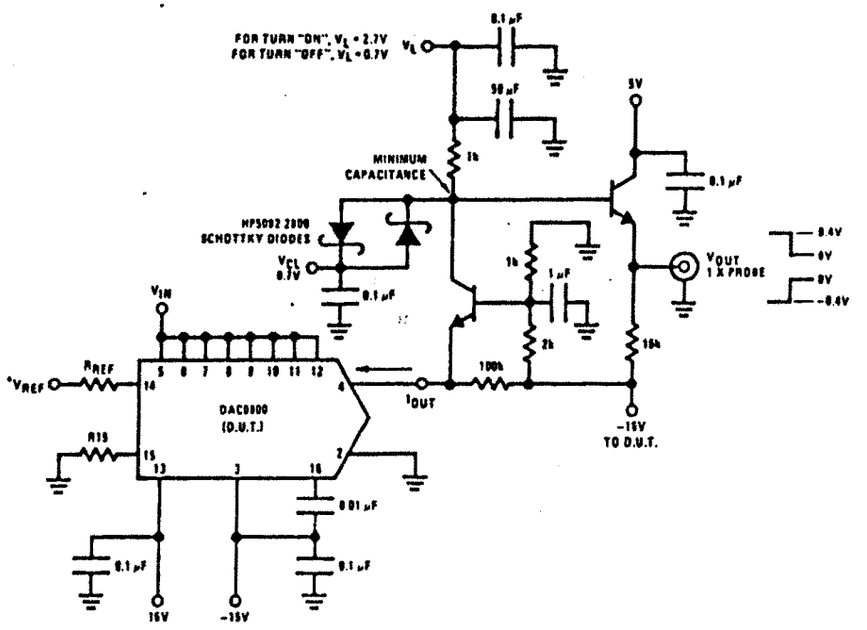

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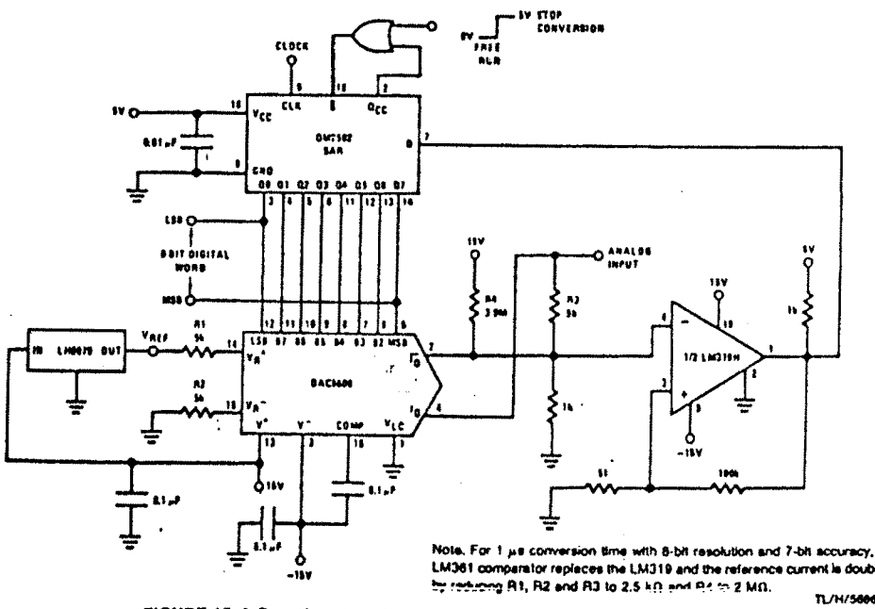
FIGURE 14. Settling Time Measurement



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

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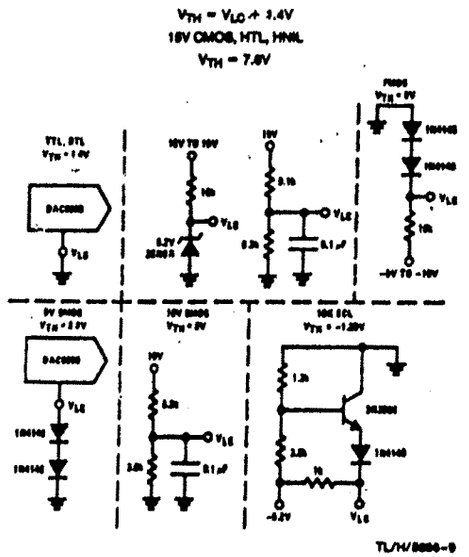
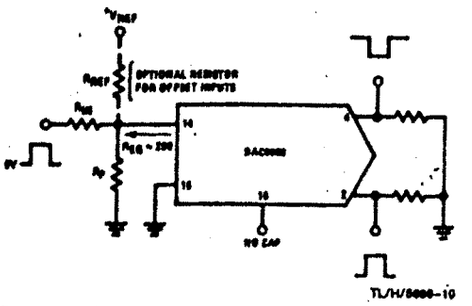
FIGURE 15. A Complete 2 μs Conversion Time, 8-Bit A/D Converter

Typical Applications (Continued)



Note. Do not exceed negative logic input range of DAC.

FIGURE 11. Interfacing with Various Logic Families



Typical values: $R_{IN} = 5k$, $+V_{IN} = 10V$

FIGURE 12. Pulsed Reference Operation

(a) $I_{REF} \geq$ peak negative swing of I_{IN}

(b) $+V_{REF}$ must be above peak positive swing of V_{IN}

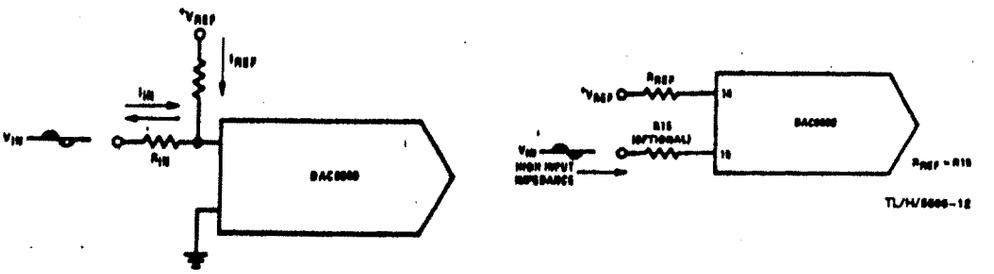


FIGURE 13. Accommodating Bipolar References

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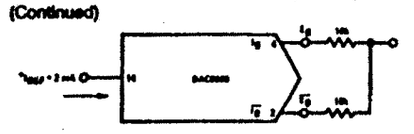
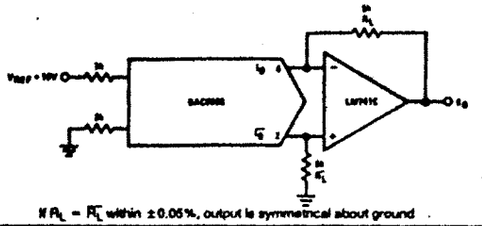
Typical Applications (Continued)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$E_{\overline{O}}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

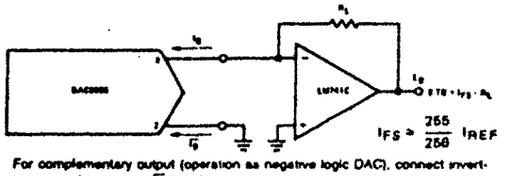
FIGURE 7. Basic Bipolar Output Operation



If $R_L = R_{\overline{L}}$ within ±0.05%, output is symmetrical about ground

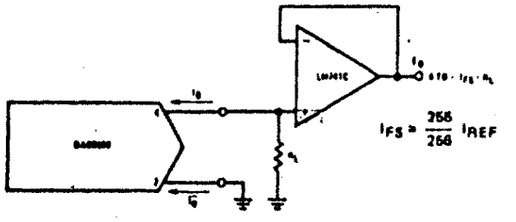
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−)Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.920

FIGURE 8. Symmetrical Offset Binary Operation



For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

FIGURE 9. Positive Low Impedance Output Operation



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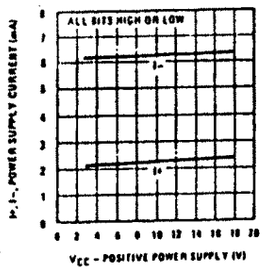
For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

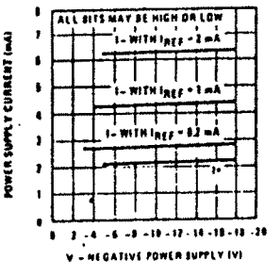
FIGURE 10. Negative Low Impedance Output Operation

Typical Performance Characteristics (Continued)

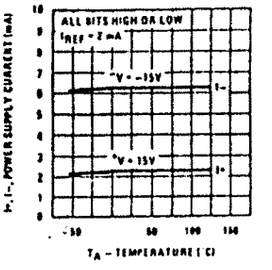
Power Supply Current vs + V



Power Supply Current vs - V



Power Supply Current vs Temperature



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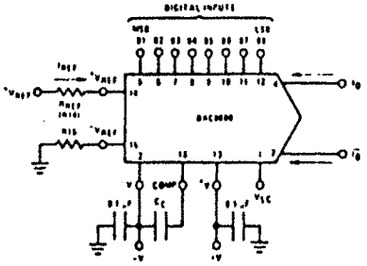
Typical Applications (Continued)



$I_{FS} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$

$R_{REF} = 5.000k$

$R15 = R_{REF}$

$C_C = 0.01\ \mu F$

$V_{LC} = 0V$ (Ground)

FIGURE 3. Basic Positive Reference Operation

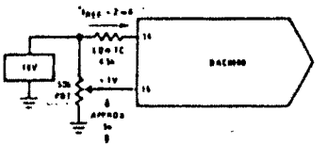
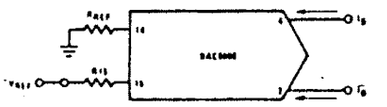
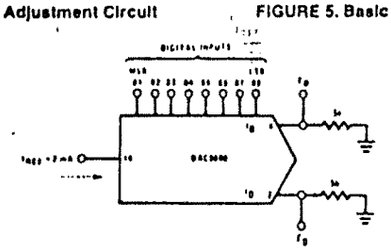


FIGURE 4. Recommended Full Scale Adjustment Circuit



$I_{FS} = \frac{V_{REF}}{R_{REF}} \times \frac{255}{256}$ Note: R_{REF} sets I_{FS}; R15 is for bias current cancellation

FIGURE 5. Basic Negative Reference Operation



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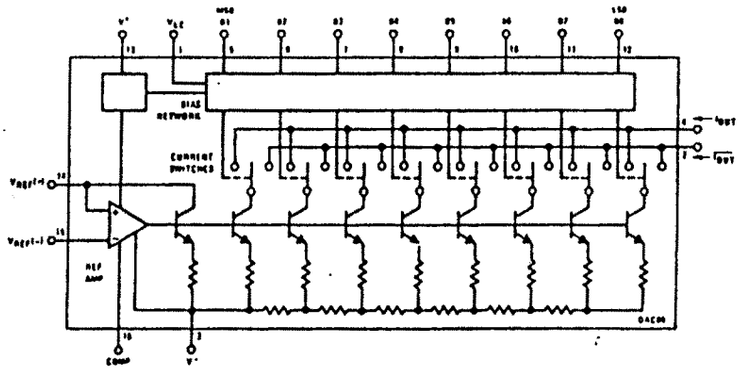
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

FIGURE 6. Basic Unipolar Negative Operation

Block Diagram



Equivalent Circuit

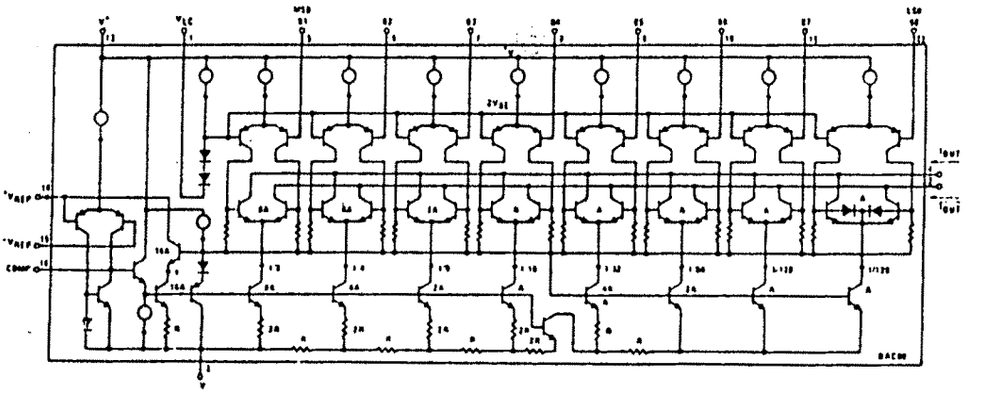


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FIGURE 2

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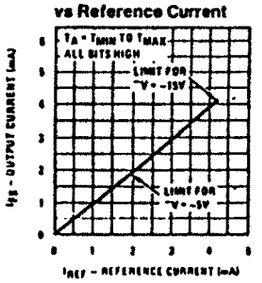
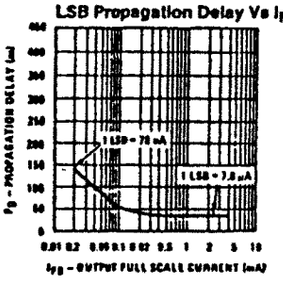
Typical Performance Characteristics

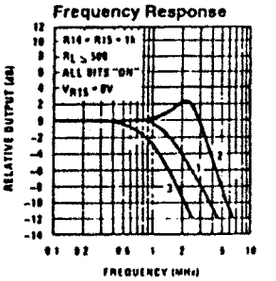
Full Scale Current vs Reference Current



LSB Propagation Delay Vs I_{FS}

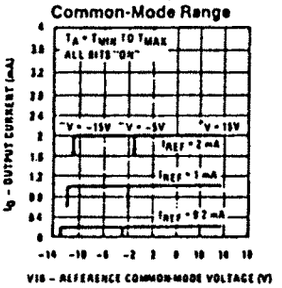


Reference Input Frequency Response



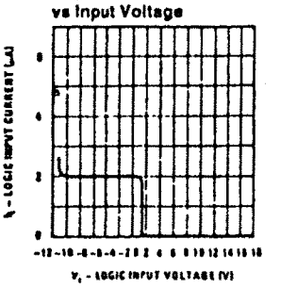
Curve 1: C_C = 15 pF, V_{IN} = 2 Vp-p centered at 1V.
Curve 2: C_C = 15 pF, V_{IN} = 50 mVp-p centered at 200 mV.
Curve 3: C_C = 0 pF, V_{IN} = 100 mVp-p at 0V and applied through 50 Ω connected to pin 14.2V applied to R14.

Reference Amp Common-Mode Range

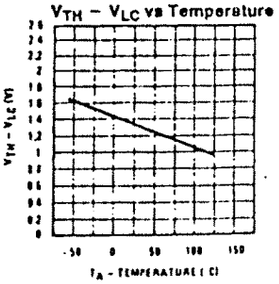


Note. Positive common-mode range is always (V+) − 1.5V

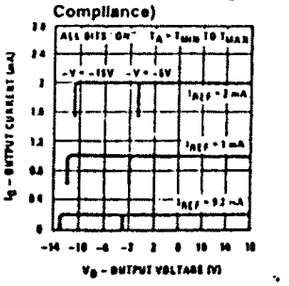
Logic Input Current vs Input Voltage



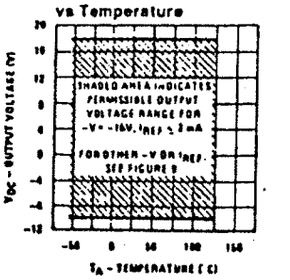
$V_{TH} - V_{LC}$ vs Temperature



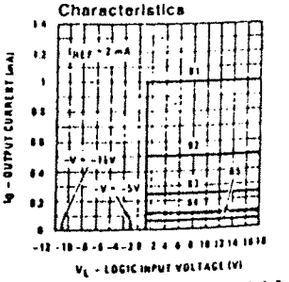
Output Current vs Output Voltage (Output Voltage Compliance)



Output Voltage Compliance vs Temperature



Bit Transfer Characteristics



TL/H/5686-3

Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ± 100 mV from actual threshold. These switching points are guaranteed to be between 0.8 and 2V over the operating temperature range (V_{LC} = 0V)