CHAPTER - III

SYSTEM DESIGN CONSIDERATIONS

CHAPTER - THREE

SYSTEM DEIGN CONSIDERATIONS

3.Ø INTRODUCTION

The principal advantage of the computer in the instrumentation system design is that to eliminate the drift of analog computer. Furthermore, the changes in designing are not a cause for total redesign of the system. With the analog circuit, once the design is determined, it is final because of the difficulty in redesigning of the PCBs. If an improvement is contemplated or we find an unanticipated "glitch" in the design, then a complete redesign of the PC board may be necessary unless we opt for unprofessional and not very elegant solution called kluge board. With the computer based design, however, many changes are possible with little or no changes in the hardware: all changes are made in the software.

In computer based system, or any industrial products, the basic function of analog input system which is interfaced to the computer is that to convert the analog input into its equivalent digital value. This function is termed as "Analog to Digital Conversion". To perform this transformation apart from the main converter many other functional blocks are required. These are an amplifier, multiplexer, signal conditioning circuits etc. The choice of these various blocks and their specifications have to be properly matched to get the optimum performance.

Analog to digital converter (ADC) choice is one of the very important consideration. In wide ranging applications,

different A/D conversion techniques are used. Flash converter, successive approximation, integrating, tracking and floating point are some of the commonly used techniques.

Class of converters known as integrating type operates on an indirect conversion method. In this method, there are many variations. But the most popular of these variations is dual slope. Though this method is rather slow, has good linearity characteristics with the capability of rejecting input noise. Low cost, makes it even more attractive. Thus the slow measurement in the laboratory and industry exclusively use this technique. So I used "Dual integration type A/D Converter" to measure millivolt and milliamperes input signals with the help of IBM PC/XT/AT. This is a mV and mA input measurement card.

3.1 mV/mA INPUT CARD

This mV/mA input card is used for the measurement of both, voltage as well as current. In the case of current measurement it accepts milliamperes input and converts it to proportional millivolt signal for measurement. The hardware is designed in such a way that it becomes ideal for many applications requiring external triggering, periodic triggering and software triggering. All the flexibilities of the A/D converter 7109 are made available through 8255 programmable input/output ports.

Speed of the dual slope converter is principally limited by the response time of the comparator, keeping in mind that the input to the comparator is a shallow ramp rather than a clean voltage steps. IC 7109 has comparator gain/bandwidth product of about 200 MHz. This mV/mA input card is not intended for fast

applications. But, with 7109 LSI chip, this card would be one of the most versatile and cost effective A/D converter on IBM-PC/XT/AT.

For external triggering optically isolated input is provided. This could be very useful in an industrial environment. Similarly, 8253 timer provides three cascadable timers, helping the user to take periodic measurements. Design of card, also offers a flexibility to detect end of A/D conversion by polling or by interrupt. Additional features like amplifier gain selection, in put filter, input over voltage protection make the millivolt and milliamperes measurement very convenient and simple for many application areas.

3.2 APPLICATION AREAS OF INPUT-CARD

The features of mV/mA input card are suitable for many applications. Some of the main applications are discussed below.

A) PERIODIC MEASUREMENT :

From the interface connector external clock can be fed to the 8253 timer. This clock frequency can be varied to control the rate of automatic samples to be taken. If desired the sampling rate can be changed under software control depending on other condition. On board timer can be used simply to generate periodic interrupts and indicating A/D conversion.

B) INTERLOCKING AND EVENT TRIGGERED MEASUREMENTS :

An input requesting to take action can automatically trigger A/D conversion cycle. At the end of the conversion the interrupt

service routine can check the analog input command deflection and the analog input value are made available simultaneously by this input card. This kind of interlocking is desirable in many industrial applications.

C) CURRENT LOOP RECEIVER :

The milliamperes ampere input card can be used as Ø-2Ø mA current loop receiver card. Input filter and over voltage protections can enable this card to reliably transfer the distant analog input information to the computer. It can used with 4-2Ø mA current loops also.

D) SENSOR INTERFACE :

Many sensors providing millivolt or milliamperes outputs can be interfaced to this card. Because of the amplifier gain selection facility, the card can accepts wide ranging inputs. The differential input of 71Ø9 lends itself to measurement of over range detection facility, sensor open condition can also be sensed.

3.3 FEATURES OF mV/mA INPUT CARD

i) 12 bit binary (plus polarity and outer range) Analog to digital converter operates at up to 7.5 conversions per second.

ii) A/D conversion can be done in EXTERNAL MODE or TIMER TRIGGER MODE or CONTINUOUS MODE.

iii) Facility for generating interrupt at the end of A/D conversion.

iv) Two interrupt generating logic blocks with interrupt level selection.

v) Opto isolator for generating trigger pulse.

vi) 16 differential Analog input channels.

vii) DIP switch for Base Address selection.

viii) DIP switch for Amplifier gain selection.

ix) Software generated " Trigger " signal for monoshot mode of 8253 IC.

x) One channel of 8253 has Interrupt generation capability.

3.4 BLOCK DIAGRAM

We know about the Intel's 8255 and 8253 data sheets and Intersil's 7109 ADC data sheet. Address decoding and control signals are generated from the control block. In case of hardware (switch) address setting and software address selection match, appropriate action is initiated. Fig.(3.1) shows the block diagram of mV/mA input card.

One of the sixteen analog input is selected using multiplexer 4051. This signal is fed to A/D converter 7109 as analog input voltage through controlled amplifier for conversions. Conversion can be done in CONTINUOUS MODE or TIMER MODE or TRIGGER MODE. Inverted output of opto isolator is used as end of conversion in TRIGGER MODE. Converted digital equivalent of input voltage can be read through Programmable Peripheral Interface (8255). After conversion interrupt can be generated by interrupt logic.

3.5 SPECIFICATION OF INPUT CARD

a) Analog Input voltage range : 0 to +/- 40.96 mV
0 to +/- 409.6 mV
0 to +/- 4.906 V

b) Analog Input current range : 0 to +/- 1 mA
0 to +/- 10 mA

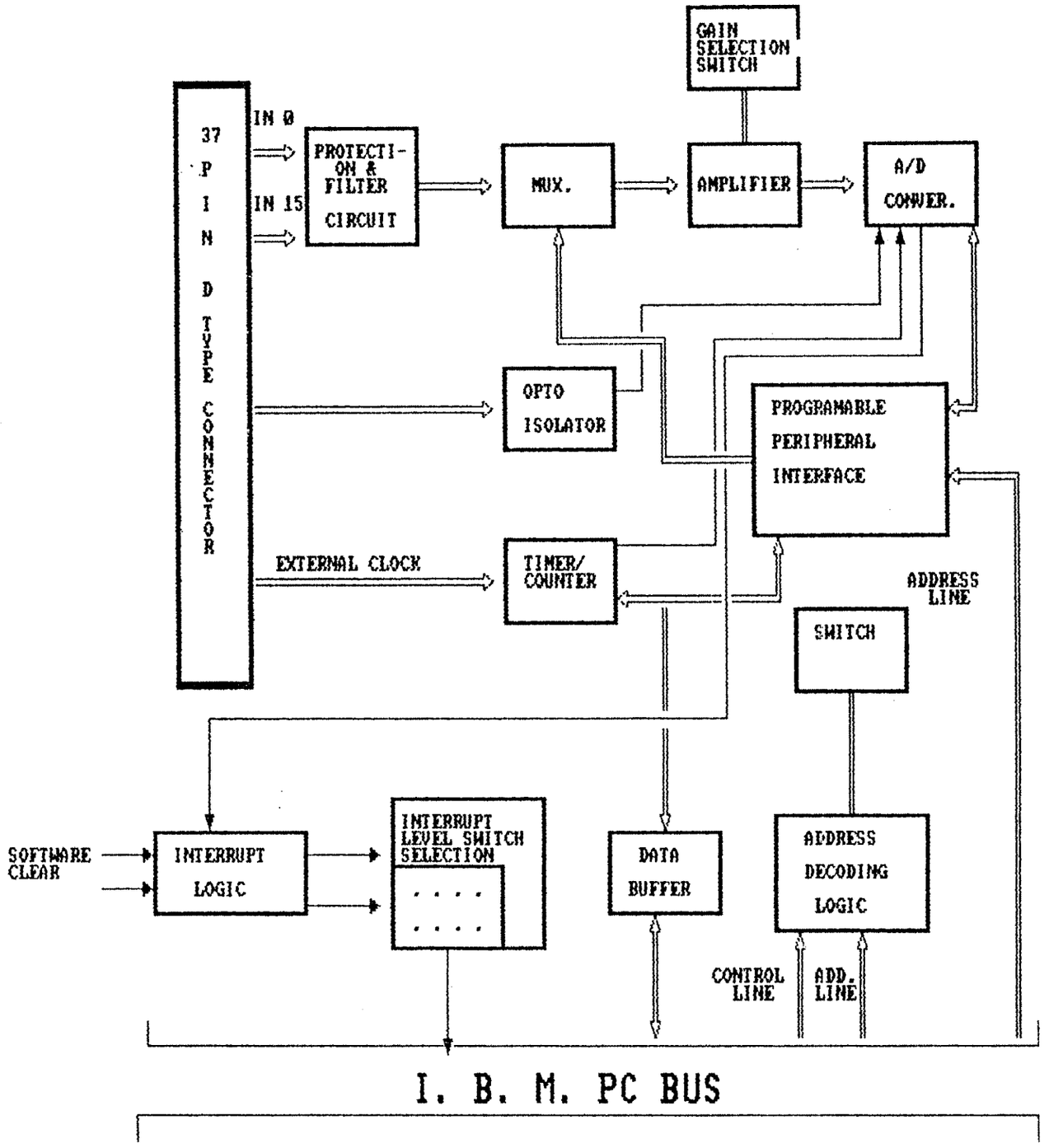


FIG . (3.1) BLOCK DIAGRAM OF INPUT CARD.

Ø to +/- 1ØØ mA

c) Resolution : 12 bits

d) Conversion time : 133 ms

e) ADC type : Dual slope integrating

f) Linearity better than Ø.Ø25% full scale (for gain =1)

g) Accuracy +/- Ø.1% at 25 degree centigrade (for gain =1)

h) Opto input current : 1Ø mA minimum

5Ø mA maximum

i) TIMER/COUNTER : frequency DC to 2.4 MHz

J) Current requirement : +5 V 3ØØ mA

+12 V 3Ø mA

-12 V 15 mA

k) Dimensions : 3Ø5 mm (L) * 1Ø2 mm (W)

3.6 HARDWARE DETAILS

Although a block diagram is quite useful to become acquainted with the overall structure of a mV/mA input card. But for detailed understanding the working of this card, it is essential to discuss the details in the circuit diagram. Here these details are discussed blockwise. It is very difficult to discuss all the circuitry in a single circuit diagram. So blockwise discussion is carried out.

3.6.1 INTERRUPT LOGIC DETAILS - After converting the ANALOG input to DIGITAL, the STATUS of ADC 71Ø9 will become low. This signal is used to interrupt the processor by using a D FLIP-FLOP. The interrupt enable input (ENI) on D is transferred to Q output after A/D conversion. By selecting any one of the interrupt level the processor can be interrupted. The 74LS74A dual edge - trig-

gered - flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and -Q outputs. Information at input D is transferred to the Q output on the positive - going edge of the clock pulse. Clock triggering occurs at a voltage levels of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

When the ADC 7109 is running in TIMER MODE after time out, interrupt can be generated by using another D FLIP-FLOP. Any one of the interrupt level can be selected by DIP switches. Table for interrupt level switch setting is given below.

Interrupt depends on STATUS:

SWA 1	ON	IRQ2
SWA 2	ON	IRQ3
SWA 3	ON	IRQ4
SWA 4	ON	IRQ7

Interrupt after TIME OUT :

SWA 5	ON	IRQ2
SWA 6	ON	IRQ3
SWA 7	ON	IRQ4
SWA 8	ON	IRQ7

SEL 3, SEL 4, interrupt Flip-Flop clear input (pulse).

Figure (3.2) shows the Interrupt Logic Details.

3.6.2 TIMER LOGIC DETAILS -By proper switch setting external clock or system clock can be used as CLK input for counter zero. Output of counter one or counter two can be used as start of conversion for ADC 71Ø9 in TIMER-MODE. It can be also used for generating interrupt. Here 8253 can be used as a counter/timer. The Intel microcomputer peripheral. It uses NMOS technology with a single +5 V supply and is packed in a 24-pin plastic DIP. It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.

SYS CLK: system clock (2.4 MHz for IBM-PC)

SEL 2: 'GATE' PULSE for counter 2 generated by software.

The fig.(3.3) shows the Timer Logic Details.

3.6.3 OPTO DETAILS - OPTO is used to run the ADC 71Ø9 in TRIGGER MODE. Input for opto is to be given through 37-pin D type connector (i.e. TRGH & TRGL input). If proper input polarity at TRGH, TRGL have been given, the output TRIG signal will be low and it will stop the conversion. When the input signal is removed, the TRIG signal will be high and conversion begins.

Opto ' MCT 2E ' is used to run the ADC 71Ø9 in TRIGGER MODE. Fig.(3.4) shows the Opto Details for producing TRIG signal.

3.6.4 AMPLIFIER GAIN SELECTION DETAILS - Amplifier gain can be selected using SWD dip switches. There are four SWD dip switches.

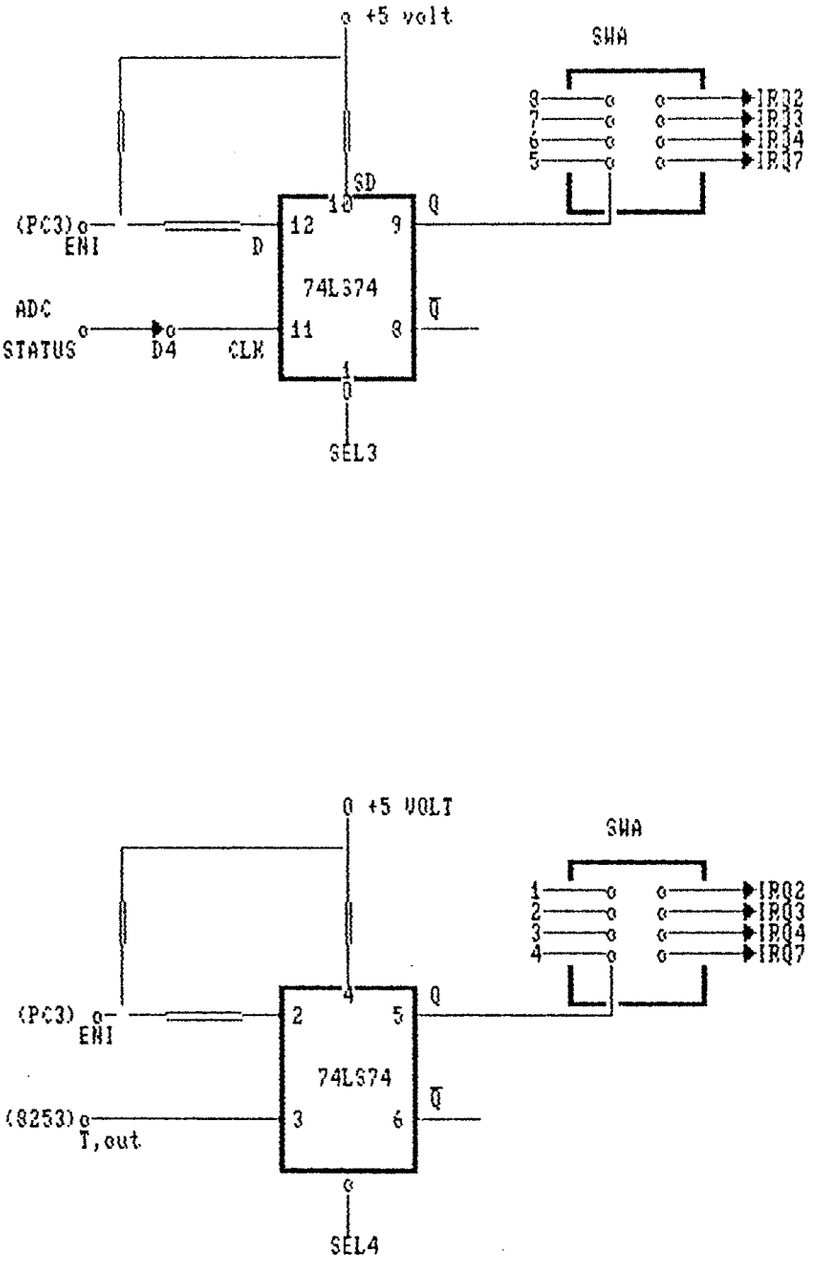


Fig.(3.2) INTERRUPT LOGIC DETAILS.

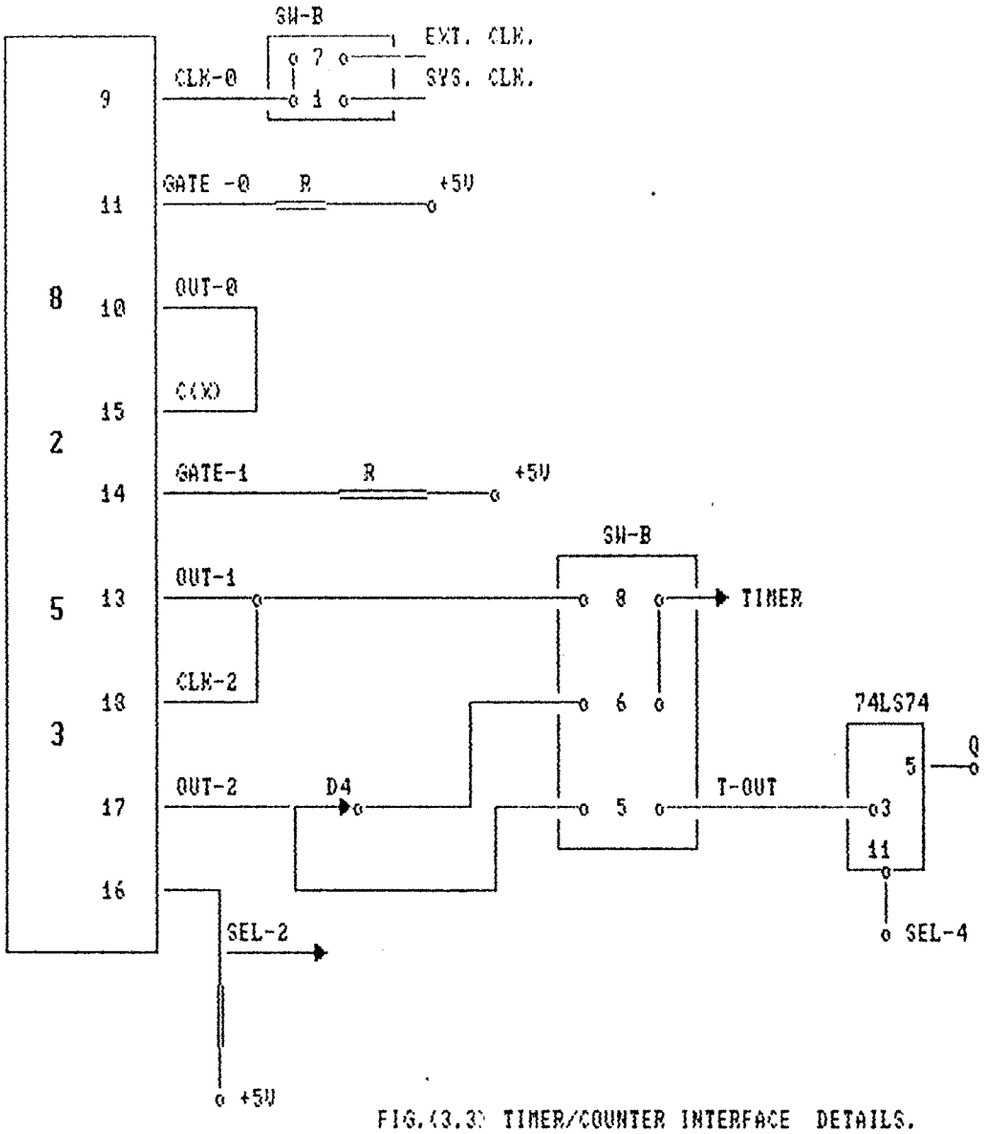


FIG.(3.3) TIMER/COUNTER INTERFACE DETAILS.

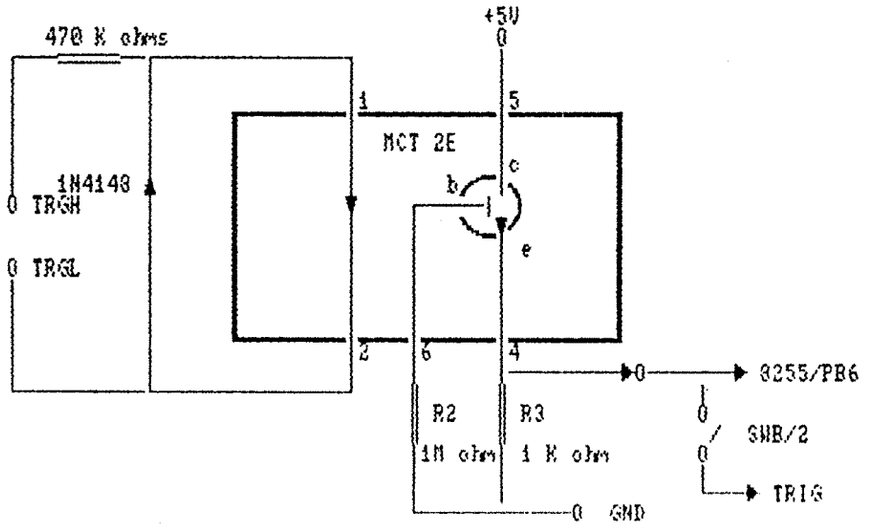


FIG.(3.4) OPTO DETAILS FOR PRODUCING TRIG SIGNAL.

These are SWD1, SWD2, SWD3 & SWD4. But for amplifier gain selection purposes SWD3 & SWD4 are not used. We have to select the gain in three forms. These are 1, 1Ø and 1ØØ. Following Table shows the selection of gain according to switch condition(ON or off).

GAIN	SWD1	SWD2
1	OFF	OFF
1Ø	ON	OFF
1ØØ	OFF	ON

3.6.5 PPI 8255 AND ADC 71Ø9 INTERFACE DETAILS -

The programmable peripheral IC 8255 plays a major role of interfacing the IC 71Ø9 to the computer. The Intel 8255 is a general purpose programmable I/C device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE Ø), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus and 5 lines, borrowing one from the other group, for handshaking.

Data Bus Buffer: This 3-state bidirectional 8-bit buffer is used to interface the 8255 to the system data bus. Data is transmitted

or received by the buffer upon execution of input or instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic: It manages all of the internal and external transfers of both data and control or status words. It accepts inputs from the CPU address and control busses and in turn, issues commands to both of the control groups.

Control Groups: In 8255 there are **Group A and Group B** controls The functional configuration of each is programmed by the system software. In essence, the CPU outputs a control word to the 8255. The control contains information such as mode, bit set, bit reset, etc.; that initializes the functional configuration of the 8255. Each control group accepts commands from the Read/Write control logic, receives control words from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A & Port C upper

Control Group B - Port B & Port C lower

The Control Word Register can only be written into. No Read operation of the Control Word Register is allowed.

Port A, B and C - The 8255 contains three 8-bit ports (A,B,C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or personality to further enhance the power and flexibility of the 8255.

Port A - One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B - One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C - One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input).

This port can be divided into two 4-bit under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

ADC 71Ø9 -The IC 71Ø9 is a high performance low power integrating A/D converter designed to easily interface with microprocessor. The output data (12-bits, polarity and over range) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A handshake mode is provided to allow the ICL 71Ø9 to work with industry-standard in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

The ICL 71Ø9 provides with high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1 μV/deg. Celsius; maximum input bias current of 1Ø pA and typical power consumption of 2Ø mW make the ICL 71Ø9 an attractive per-channel alternative to analog multiplexing for many data acquisitions.

Low order 8-bit data of ADC 71Ø9 are connected to Port A. Higher order 4-bits are connected to port B. Polarity, status and over range are also connected to PB5, PB7 and PB4 respectively. Lower byte can be read outputting active low LBN signal. Higher byte can be read by low HBN signal. PC2 of 8255 can be

programmed to RUN the ADC 7109 in **CONTINUOUS MODE**. If ADC 7109 is running in **TRIGGER MODE** its status can also be read via PB6.

Fig.(3.5) shows the PPI 8255 - ADC 7109 **INTERFACE DETAILS.**

3.6.6 MULTIPLEXER CONFIGURATION DETAILS - Multiplexer used in this mV/mA input card are CD 4051 BM single 8-channel multiplexers. Here four multiplexers are used. These analog multiplexers are digitally controlled by analog switches having low "ON" impedence and very low "OFF" leakage currents. Control of analog signals up to 15 Vp_p can be achieved by digital signal amplitudes of 3-15 V.The 4051 is a single 8-channel multiplexer having three binary control inputs. A, B, C and inhibit Input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output. An inhibit pin which when held high disables outputs. If we are going to use 3 or 4 analog channels then the common input terminal along with the input pin is grounded.

In this card each channel contains a 50 Hz single pole low pass filter as standard input configuration. This frequency can be easily changed or the filter can be removed entirely. Fig.(3.6) shows the MUX. Input circuit. In filter circuitry two Zener diodes of 9.1 Volts are connected back to back in parallel with the 1MFD capacitor of 100 V. This is a protection circuitry for each channel of the multiplexer. Output of each input circuitry is connected to the proper channel of the multiplexer. Here two pairs of 4051's are used for 16 channel purposes. In one pair, one mux. is used for high input and another mux. is used for low input.Selected inputs of MUX. have connected to the

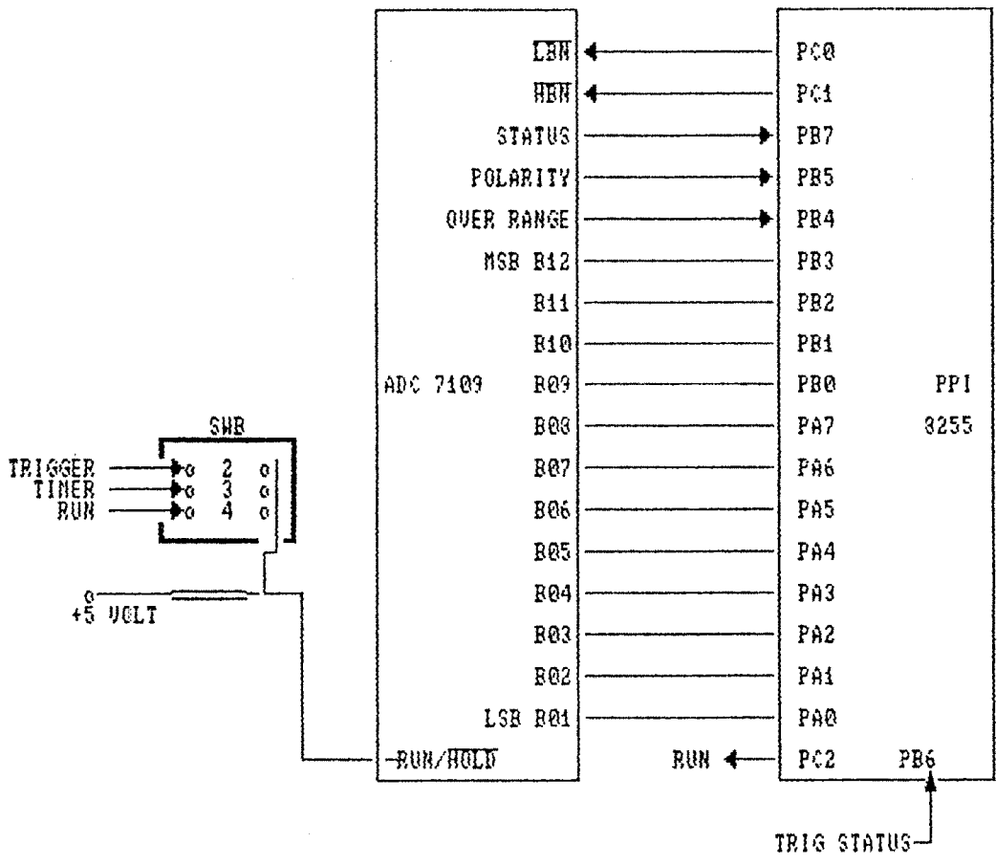


FIG. (3.5) 8255 ADC 7109 INTERFACE DETAILS

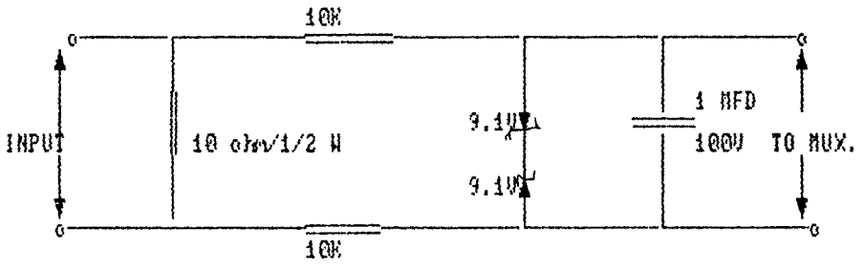


FIG. (3.6) THYE MUX INPUT CIRCUIT.

higher nibble of port c as shown in the figure. The user can program 8255 to select any one of the 16 differential analog input channels. Fig. 3.7 shows the 16-channel MUX. configuration details.

3.6.7 INTERFACING DEVICES - Several types of interfacing devices are necessary to interconnect the components of a bus oriented system. The devices used in todays microcomputer system are designed using Large scale Integration (LSI) technology. In addition, tri-state devices are essential to proper functioning of the bus-oriented system, in which the same bus lines are shared by several components.

A) Octal Bus Transceiver with 3-state output (74LS645) : Tri-state logic devices have three states: logic 1, logic Ø, and high impedance. A tri-state logic devices has a third line called an Enable. When this line is activated, the tri-state device functions the same way as ordinary logic devices. When the third line is disabled, the logic device goes into a high impedance state as if it were disconnected from the system. Ordinarily, current is required to drive a device in logic Ø and logic 1. In the high impedance state, practically no current is drawn from the system.

The 74LS645 octal bus transceiver is used for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. This allow data transmission (for e.g. from the A bus to the B bus or from the B bus to the A bus) depending up on the logic level of the direction control input. Enable input can disable the device so that the buses are effectively isolated.

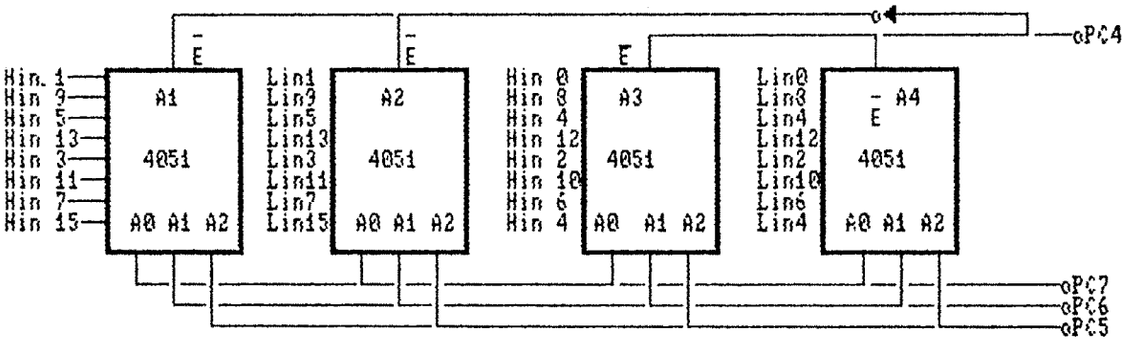


FIG.(3.7) 16- CHANNEL MUX. CONFIGURATION DETAILS.

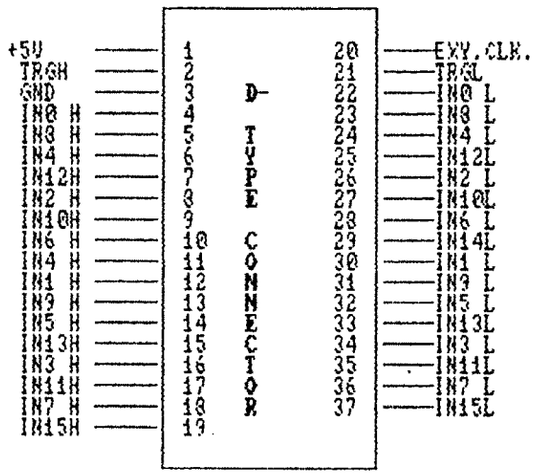


FIG.(3.8) CONNECTOR PIN CONFIGURATION.

B) DECODER (74LS138 1-of-8 Decoder) : The decoder is a logic circuit that identifies each combination of the signals present at its input. The 74LS138 is a high speed 1-of-8 decoder. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138 and inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

C) Hex Inverter (74LSØ4): It is a low power Schottky hex inverter IC. It is used in logic circuitry at the output of the 74LS138 decoder. This IC consist of six inverter, so it is called the Hex Inverter. Maximum supply voltage for this IC is 5.25 V. Its 'Operating Ambient Temperature Range is' between -55 to 125 deg. Celsius.

D) Quad 2- Input AND Gate (74LSØ4)' : It is also a low power schottky quad 2-input AND gate. It consist of 4 AND gates in a single package, there fore it is called the 'Quad 2-input AND Gate'.

E) 4-Bit Magnitude Comparator (74LS85) : The 74LS85 is a 4-bit magnitude comparator which compares two 4-bit words (for e.g. A,B), each word having four Parallel Inputs ($A_Ø$-A_3, $B_Ø$-B_3); A3, B3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monolithic code. **Three outputs are provided** :' A greater than B' (OA>B),' A less

than B' (OA<B),' A equal to B' (OA=B). Three expander Inputs, IA>B, IA<B, IA=B, allows cascading without external gates. Four proper compare operation, the Expander Inputs to the least significant position must be connected as: IA<B=IA>B=L, IA=B=H. For serial expansion, the OA>B, OA<B & OA=B outputs are connected respectively to the IA>B, IA<B, and IA=B inputs of the next most significant comparator.

3.6.8 BASE I/O ADDRESS SELECTION : For interfacing an 'Input card' to the PC I/O mapped I/O can be used and linear select decoding can be used to reduce the cost of the hardware. Base address selection logic details are tabulated below. All the combination of the switches SWC 1-4 are supported by the card. For SWITCH ON=Ø & SWITCH OFF=1.

Address Selection Form	SWC1 A_6	SWC2 A_7	SWC3SWC4 A_8	A_9
24Ø	1	Ø	Ø	1
28Ø	Ø	1	Ø	1
2CØ	1	1	Ø	1
34Ø	1	Ø	1	1

3.6.9 REGISTER DETAILS FOR SOFTWARE : The address of each registers of 8255 and 8253 with respect to selected base address are explained below. The two interrupt generating FLIP-FLOPS require one address location each.

Base address is selected by DIP SWITCH.

[BASE + Ø]	RD	8255	PORT A
[BASE + 1]	RD	8255	PORT B
[BASE + 2]	WR	8255	PORT C
[BASE + 3]	WR	8255	CONTROL REGISTER
[BASE + 4]	WR	8253	LOAD COUNTER Ø
	RD	8253	READ COUNTER Ø
[BASE + 5]	WR	8253	LOAD COUNTER 1
	RD	8253	READ COUNTER 1
[BASE + 6]	WR	8253	LOAD COUNTER 2
	RD	8253	READ COUNTER 2
[BASE + 7]	WR	8253	CONTROL REGISTER
[BASE + 8]	SEL2		Pulse generated to trigger the 'Gate' of 8253 COUNTER 2
[BASE + 12]	SEL3		To generate conversion over interrupt flip-flop clear
[BASE + 16]	SEL4		To generate timer interrupt F-F clear

3.6.1Ø AMPLIFICATION AND PRESET ADJUSTMENT : The gain of amplifier can be adjusted to offer specified performance. From some sensor outputs if gain is to be changed using Preset PR4, also offset adjustment is to be done with PR3. The full scale input adjustment can be done by changing the reference of 71Ø9, that is by adjusting PR2. This adjustment may result in loss of linearity.

Some bridges like strain gauge have very low output voltages. The input noise of 71Ø9 itself is about 2Ø micro-volt peak

to peak. The microvolt output of the bridge should be amplified by low drift, low offset operational amplifier LF 356. Averaging several conversions with the help of SOFTWARE would reduce the effects of the jitter.

3.6.11 37 PIN D-TYPE MALE/FEMALE CONNECTOR : The 37 pin connector is used for connecting the outputs of signal conditioner. In this system we can use 16 channels, these are 'INØ-IN15'. Each input channel consists of two wires for connecting low and high signals. Low signals are 'INØL-IN15L' and high signals are 'INØH-IN15H'.

Here 32 pins are used for connecting the outputs of the signal conditioner to the inputs of the INPUT CARDs filter circuitry. Two pins are connected to the trigger high (TRGH) and trigger low (TRGL) inputs. If external clock is required then one pin is connected to the EXT.CLK. circuit. Remaining two pins are used for +Vcc and ground (GND). Fig.(3.8) shows the connector pin configuration.

3.7 SYSTEM DESIGNED APPLICATIONS

The advent of modern digital computers has great impact on the modern human civilization. The impact which is not considered in the world only but has extended into the numerous fields as well. Usually one comes across the term "data processing " in the field of computer science. The data processing concerns with processing, which may be either scientific or nonscientific, of the information to draw some conclusion, to establish some theories or to study a subject thoroughly.To achieve such task one

has to have the information, not in little amount but in huge amounts. So the information, or in more meaningful word, the data has to be collected under various conditions. Therefore one should have a system which will collect or more specifically acquire the data and will make it available to the user for his various interest. Such system is the "data acquisition system". My attempt is to design a multichannel DAS which will acquire the data along multiple paths or channels simultaneously.

The task of collecting the data is done by the system for four major applications. These are -

i) Temperature measurement;

ii) To find the electrical field for conductivity measurement;

iii) Thermoelectric power measurement and

iv) Semiconductor characteristics (for e.g. Diode) measurements.

For different analog inputs such as temperature, voltage, current etc. different signal conditioning circuits are used.

3.7.1 TEMPERATURE MEASUREMENT

In this system one channel is used to measure the temperature for plotting the graph of temperature against time. In the temperature sensing circuit, LM 335 can be used as a temperature sensor. The fig.(3.9a) shows the block diagram of this system.

This system is a composed of a temperature sensor (LM 335), amplifier (op-amp 741), input card for interfacing (mV/mA input card) and the computer. Fig.(3.9b) shows the schematic diagram, which is designed for the temperature sensor and amplifier. This circuit is designed for the temperature range Ø to 1ØØ

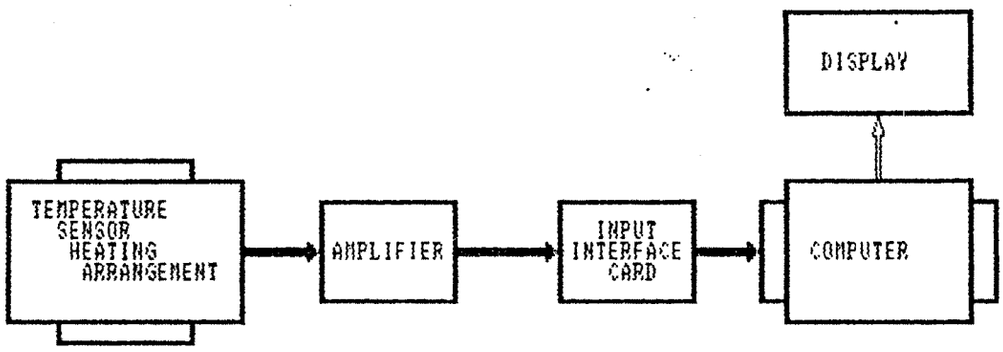


FIG.(3.9a) TEMPERATURE MEASUREMENT BLOCK DIAGRAM.

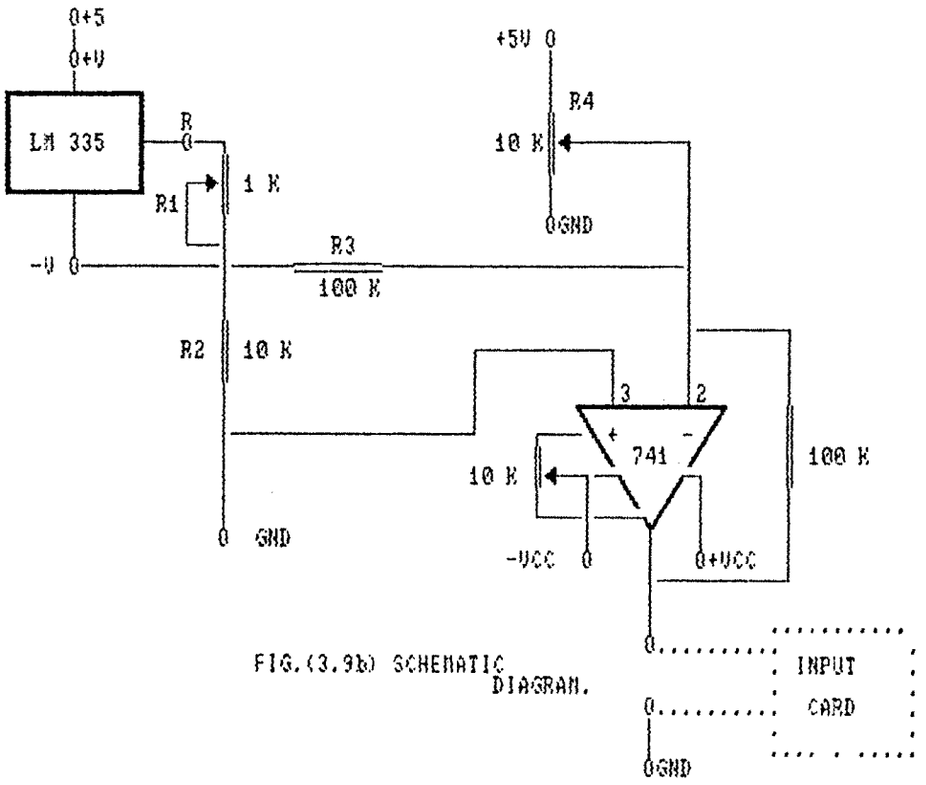


FIG.(3.9b) SCHEMATIC DIAGRAM.

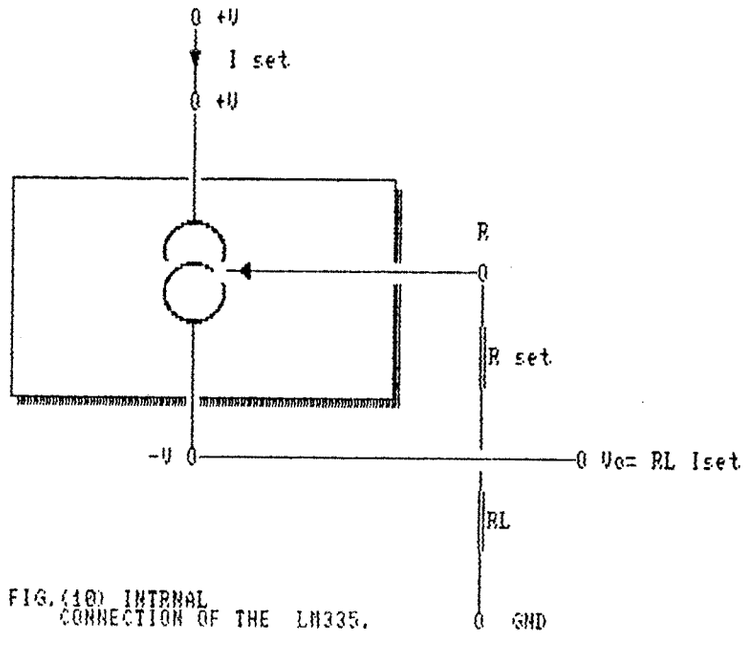


FIG.(10) INTRNAL CONNECTION OF THE LM335.

deg.Celsius. The output of the temperature sensor changes linearly as a function of temperature (10mV/deg.Celsius). This output is an input to the amplifier, which is used to calibrate the output of the temperature sensor for a desired temperature type (Kelvin, deg.Celsius or deg.F.). Potentiometer R4 is adjusted so that a suitable voltage appears at the output of the amplifier. Since the output of temperature sensor is directly proportional to temperature changes, R4 needs to be adjusted at only one temperature. Here offset can be adjusted by using the preset, R6, of 10 K ohms. If the output of this amplifier is small then another amplifier can be used at its output stage in the inverting mode. The purpose of this inverting amplifier is; i) to invert the output, so that its output voltage is positive, ii) to provide suitable gain for better accuracy. The output of this amplifier is input to the " input mV/mA card ", so that input to this card is directly proportional to temperature.

The temperature sensor LM 335 is a three terminal adjustable current source whose current can be programmed from 1 microampere to 10 microampere with one external register Rset. The three terminals are labeled +V, R and -V. The internal connection of the LM 335 is shown in the fig.(3.10). It has a wide operating voltage range of 1 to 40 volts. It can also be withstand reverse voltage of up to 20 V (terminal +V is negative with respect to -V). Sensor is designed to operate over a temperature range of 0 to 70 deg.Celsius. For the other component values indicated in the schematic diagram (3.9b), the output changes 10 mV per deg. Celsius.

The mV/mA input card is interfaced to the computer and

output voltage can be recorded.

CALIBRATION: In this application of the DAS the temperature can be sensed and the graph of temperature (in deg.Celsius) against time (in second) was plotted. So that calibration is essential. For the calibration, first the experiment was done manually with heating the sensor and 25 readings of the out voltage for different temperatures in increasing order are taken. In this calibration process temperature measured up to 7Ø deg. Celsius and voltage measured up to 7ØØ mv. The graph of temperature against output voltage was plotted (temperature in deg.Celsius and o/p voltage in mV). The nature of the graph is a straight line.From this plot slope is equal to Ø.Ø722. We have the equation of straight line,

$$y = mx + c$$

where, x and y are variables,

m is the slope of the straight line

and c is the intercept.

Using this equation multiply the incoming output voltage by the slope and add the room temperature. The result is directly proportional to the temperature of the sensor with respect to time. Thus calibration can be done. Same procedure was repeated for the cooling arrangement of temperature sensor,the same result was obtained.

CONCLUSION : In this application, temperature is sensed and graph was plotted against time for both heating as well as cooling arrangement. From the graph it is seen that as the time goes on increasing temperature increases and as the time decreases

temperature also decreases.

3.7.2 ELECTRICAL FIELD FOR CONDUCTIVITY MEASUREMENT:

Electrical conductivity is an important physical property of dielectric crystal, required not only for practical applications but also for the interpretation of various physical phenomena. Valuable information about the ferroelectric property of a material can also be obtained from the studies on electrical conductivity. Ferroelectrics exhibits conduction and semiconductor effects not usually observed in insulators. The conduction mechanism in polar materials can be ionic and/or electronic in nature. Most polar dielectrical materials show only a gradual increase in conductivity with increasing with increasing temperature. However, dramatic changes have been observed in certain ferroelectric materials near their Curie point.

The d.c. electrical conductivity of a material is an intrinsic or inherent property of the material. It denotes its ability to conduct electric charge. The conductivity of a solid dielectric depends on the mobility of charge carriers and on their concentration. The conduction, however, can occur unless the charge carriers are made available for the process through activation by some external agency like thermal and electrical energies. The variation of conductivity (σ) with temperature (T) can be expressed by the general exponential relation,

$$\sigma = \sigma_{\emptyset} \exp (- E/KT)$$

where, E is the activation energy,

$\sigma_{\emptyset}$ is the constant and

K is the Boltzmann constant.

To study the variation with temperature of d.c. electrical conductivity and to understand the mechanism of potassium vanadate (KVO_3), it is essential to find the electrical field for conductivity measurement.

According to Robert's suggestion in 1975, the electrodes play an important role in the measurement of conductivity and thermoelectric power. He also reported that ohmic contact is the most essential requirement for such measurements. Therefore to ensure the ohmic contact between pellets and electrode interface, the current I through the pellet was measured as a function of applied d.c. field (E) at a constant temperature. The current density (J) was determined with the help of ($J=I/pi*r^2$) relation, where r is the radius of the pellet.

This application of data acquisition system is an attempt to find the electrical field for conductivity measurement of Potassium vanadate. This experiment is carried out at high constant temperature. Here data file is created for variation of current density (J) with the d.c. electrical field (E).From the data file the graph of current density (J) [in A/sqr.cm] is plotted against applied electrical field (E) [in V/cm]. This electrical field (E) is used for the measurement of d.c. conductivity.

EXPERIMENTAL DETAILS: Fig.(3.11) shows the block diagram of the electrical field find out for conductivity measurement system arrangement. This system is a composed of a d.c. conductivity measurement cell with heating arrangement, a transistorized power supply unit to provide d.c. electrical field, input interfacing

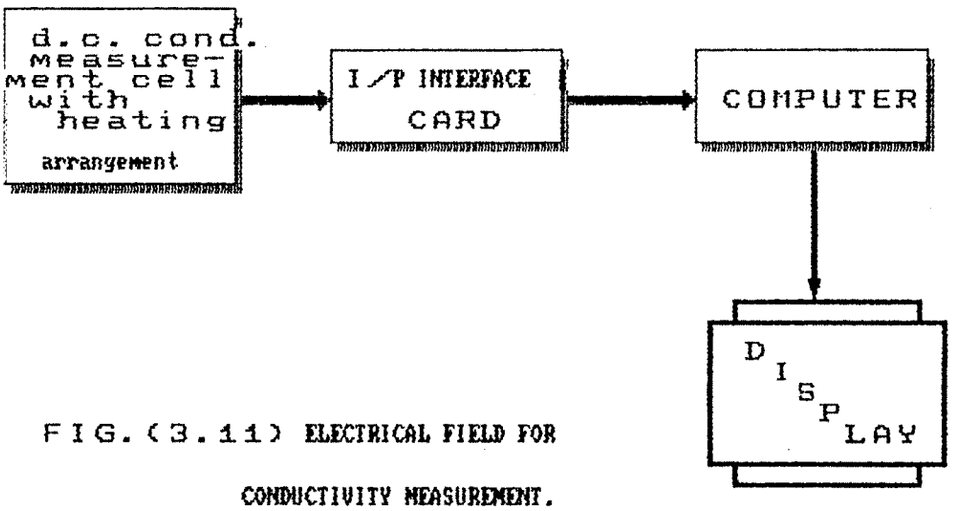


FIG.(3.11) ELECTRICAL FIELD FOR CONDUCTIVITY MEASUREMENT.

card and computer system. The flat faces of the pellet sample were made smooth and parallel. Faces were polished with an air-drying silver paste for good ohmic contact. The d.c. conductivity investigation were based on the d.c. resistivity data obtained by two probe method. Pellet mounted conductivity measurement cell is heated for high temperature (for e.g. at 300 deg.Celsius it is kept constant). Apply the electrical field to the cell, goes on increasing the field in certain steps and measure the current density (J).For this experiment two channels of DASs are used. One is for the measurement of applied electric field (E) and another is for the measurement of the current density (J).

CONCLUSION : From the plot of J versus E, it is seen that the non-linearity is observed at the lower field (E< Emin) region, which can be due to the effect of space charge built-up giving rise to non-uniformity of the field distribution between the electrodes. It was also noted that the increase of J with E becomes faster for E>Emax. So for the measurement of σ, the d.c. electrical field chosen was 100/cm, which had been applied throughout the experiment, falls within the range of ohmic contact.

3.7.3 THERMOELECTRIC POWER MEASUREMENT :

The studies on thermoelectric power gives fundamental informations regarding the mechanism of conduction in solids. The studies on thermoelectric power also give the role of different types of carriers that govern the electrical conductivity and help to decide whether the conduction is due to thermally activated hopping or not. It is also possible from this data to

compute temperature variation of fermi-level and to explain the possible forms of conduction from the impurity concentration content of the sample. Thermoelectric power gives useful information regarding the nature, the number and the effective mass of the charge carriers in solids. Together with electrical conductivity data it can yield information regarding the drift mobility of the charge carriers and the mechanism of electrical conduction in solids.

Seebeck in 1821 found that if the metal was connected at its two ends with a second metal and if one of the junction was heated, a potential difference was developed across the open ends of the second metal. This potential difference is called Seebeck or Thermoelectric emf. The potential difference is developed because more of the majority charge carries in the solid diffuse from the hot to cold junction. One of the basic thermoelectric properties of the material is thermoelectric power or Seebeck coefficient(s), which can be defined as the emf developed when a unit temperature difference exists between the points of measurement.

Heikes in 1961 reported that Seebeck coefficient(s) is independent of temperature and magnitude primarily depends on the density of the charge carriers, which is expressed by Heikes formula,

$$S = (K/e) * \log ((Ns/n)-1)$$

where n is the number of carriers in the states and Ns is the total number of available states; K is the Boltzmann constant and e is the charge on the carrier.

In the present application of data acquisition system,

an attempt has been made to study the temperature variation of thermoelectric power of:i) Lithium Vanadate ($LiVo_3$) doped with Ø.Ø25 mole % of Chromium Oxide (Cr_2O_3) and ii) Pure Lithium Vanadate ($LiVO_3$).

EXPERIMENTAL DETAILS : The fig.(3.12) shows the block diagram for the measurement of thermoelectric power at various temperatures. It consist of an electrically heated furnace, a temperature controlled arrangement, input mV/mA measurement interfacing card and the computer. A specially designed sample holder is used for the thermoelectric power measurement. Here the samples of pure Lithium Vanadete ($LiVO_3$) and Lithium Vanadete doped with chromium Oxide at concentration of Ø.Ø25 mole % were used in the form of pellets. These pellets having thickness about Ø.2 cm and diameter 1 cm were sintered, polished and coated with thin layer of air-drying silver paste for good electrical contact. The pellets are put into the sample holder for the measurement of thermoelectric power. The schematic diagram of experimental set up for the measurement of thermoelectric power is shown in fig.(3.13).

Thermoelectric power of these samples was measured by producing a thermal gradient (delta T approximately equal to 25 deg.Celsius) across the samples with the help of small heater attached to one of the hard electrodes of the sample holder. Silver electrodes were used for this measurement. The thermal gradient (delta T) was measured using chromal alumel thermocouple directly connected to the input interfacing card. Thermo emf (delta E) developed across the pellet was also connected to

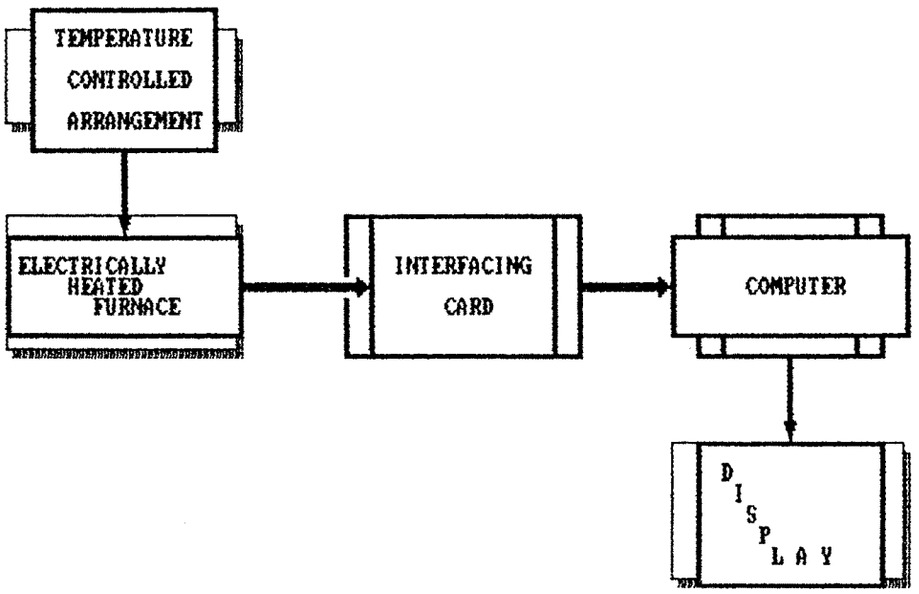
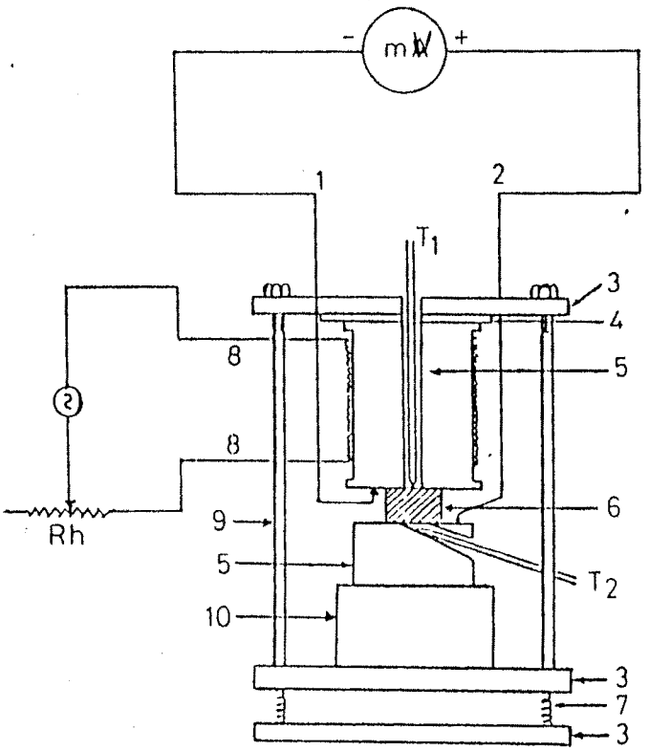


FIG.(3.12) BLOCK DIAGRAM FOR MEASUREMENT OF THERMOELECTRIC POWER.



1,2 - Silver electrodes, 3 - Metal plates, 4 - Mion sheet, 5,5 - Hard metal electrodes, 6 - Sample pellet 7 - Spring 8,8 - Sub heater leads, 9 - Metal rod, 10 - Metal block, T_1, T_2 - Thermocouples.

Fig. 3.13 - Scematic diagram of experimental set-up for the measurment of thermoelectric power.

* Here Channel Connections are -

i) ch0 = T_2 = Furnace Temperature

ii) Ch1 = mv = EMF measured

iii) ch2 = T_1 = Difference Temperature

interfacing card. Sufficient time was given after applying thermal gradient to get stability before recording the thermo emf. The samples were heated by establishing the constant thermal gradient and the developed thermo emf was measured at different ambient temperatures of the sample. Furnace temperature is also connected to the interfacing card for measurement purpose. The totally three channels were used for this experiment. Here data file can be created for the measurement of furnace temperature, thermo emf (delta E), difference temperature (delta T) and thermoelectric power. Due to the fluctuations coming from the temperature controlled arrangement and electrically heated furnace it is very difficult to adjust them properly. There fore after stability in the readings data file is prepared.

Thermoelectric power was determined by using the relation,

Thermoelectric power(S)=(delta E)/(delta T)

CONCLUSION : From the data file, graph is plotted for the temperature variation of thermoelectric power in pure lithium vanadate and lithium vanadate doped with Ø.Ø25 mole % concentration of chromium oxide. From the graph, the thermoelectric power(s) increases with increasing temperature and reaches a maximum value. After that, it start∅to decrease with increasing temperature and becomes negative with further increase in temperature. It is observed that the sign of thermoelectric power is positive in ferroelectric region of the samples, indicating that the majority charge carriers are holes. However, the sign of thermoelectric power is reversed at a certain temperature indicating the " phase transition temperature " of respective sam-

ples. The negative sign of thermoelectric power in paraelectric region of the samples reveals that the majority charges are electrons and the samples becomes n-type semiconductor. IT is therefore, concluded that the density of positive charge carriers at the transition temperature is equal to the density of negative charge carriers.

From the graph it is seen that the thermoelectric power increases with increasing temperature in ferroelectric region. This is due to increasing mobility of the charge carriers which increases exponentially with temperature. The increase in mobility of charge carriers with temperature in ferroelectric state of samples suggests a mechanism that deals with polaron hopping conduction . In hopping type conduction , polarons move from one impurity center to another by a thermal activated hopping (transfer) process and mobility of charge carriers increases exponentially with temperature.

It is also observed from the graph that the thermoelectric power decreases with increasing temperature, in high temperature region i.e. in paraelectric state which is in accordance with the normal band conduction. In the normal band conduction, the number of charge carries increases exponentially with the temperature and the mobility of charge carriers decreases with temperature. Due to these factors thermoelectric power decreases with temperature and becomes negative in the paraelectric region. The transition from the positive value of the thermoelectric power to the negative value at the curie temperature of the sample may be due to fact that mobility of the electron increases while mobility of the holes decreases in paraelectric region; which eventually

reduces the thermoelectric power and resulting there by negative charge carriers, dominating over the positive charged holes and the material becomes n-type semiconductors.

3.7.4 DIODE CHARACTERISTICS MEASUREMENTS

The action of the PN junction is the basis of the working of all semiconductor devices; e.g. P-N junction diodes, transistors, silicon controlled rectifiers, field-effect-transistors etc. Therefore it is essential to know the action of P-N junction, which is essential for all semiconductor devices. The diode characteristic measurement application of data acquisition system is an attempt to study the "P-N junction characteristics" of the diode.

Two channels of multiplexer are used to plot the characteristics of the semiconductor device, such as diode. For this application a simple forward bias circuit can be used. One channel is used for the voltage measurement and another is used for the current measurement. The fig.(3.14) shows the block diagram for the study of the forward characteristics of the diode when it is forward biased. The circuit diagram for the study of the characteristics of the diode when it is forward biased is shown in fig.(3.15). The forward voltage is increased from zero in suitable equal steps and the resulting current is recorded. The voltage is increased in steps of millivolts and current is recorded in microamperes. The data file is created for the recording of voltage as well as corresponding current. The graph is plotted for the forward current against the applied voltage.

CONCLUSION: The forward characteristics is not a straight line.

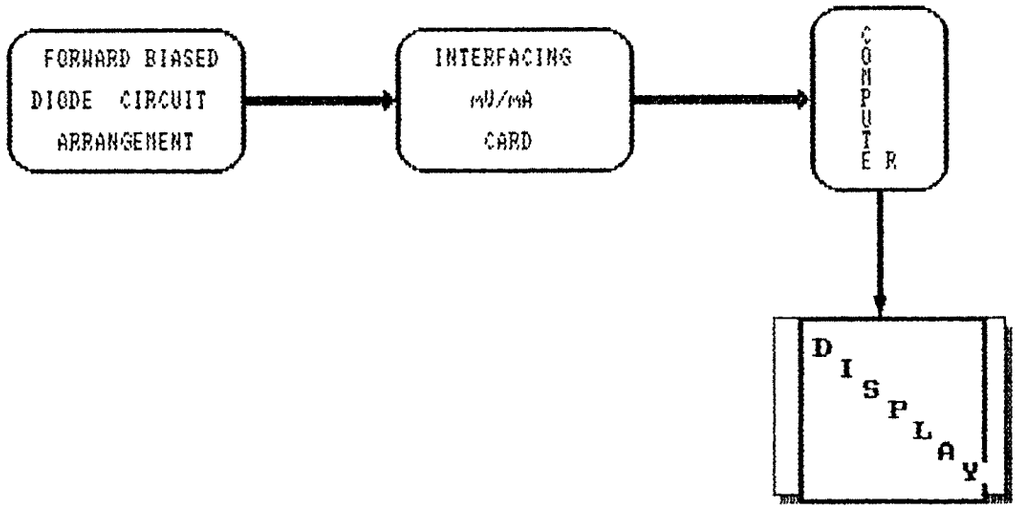


FIG.(3.14) BLOCK DIAGRAM OF THE DIODE CHARACTERISTICS MEASUREMENT.

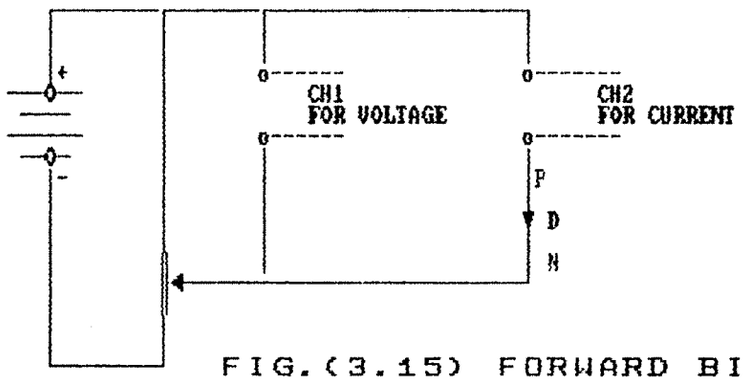


FIG.(3.15) FORWARD BIASED DIODE CIRCUIT.

Therefore, the ratio V/I is not a constant i.e. diode does not obey Ohm's law. Hence semiconductor diode is a nonlinear conductor of electricity.

For small values of the forward voltage V_F less than the internal potential barrier Vo (which is approximately Ø.3 volt for germanium diode and Ø.7 volt for silicon diode at 25 deg. Celsius), I_F is zero. This is because Vo opposes V_F and, therefore, in this case ($Vo > V_F$) the potential barrier prevents holes from P-region and electrons from the N-region to flow across the depletion region in opposite directions.

When V_F becomes greater than Vo a small current flow. The forward voltage below which I_F is zero and just above which I_F starts increasing rapidly is called the cut-in, threshold, offset or break-point voltage. The cut-in voltage is equal to the potential barrier.

As V_F is further increased the current increases very rapidly. Increase of the forward bias voltage increases the speed of the flow of electrons and holes. When the electrons moving with increased kinetic energy collide with crystal atoms, some covalent bonds of the atoms are broken. Consequently pairs of electron and hole are created. This effect increases the forward current. As the current increases the heating effect in the crystal increases. The heat is dissipated in the material so that the temperature of the material rises. Since the generation of pairs of electron and hole depends on the temperature, the rise in the temperature causes further increase in the current. Thus the whole effect is cumulative. For large values of V_F compared

to Vo the current increases exponentially with V_F. Therefore, under the forward bias condition corresponding to the steep part of the curve the PN junction diode offers low resistance to the flow of current.

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