C H A P T E R II

BACK-GROUND DISCUSSION.

Objective of the present discussion is to elaborate upon various aspects of instrumentation involved while acquising transport properties of the materials at cryogenic temperatures. Methods adopted to device cold stations, where cooling power as well as temperature of the station could be controlled are briefly discussed in Sec. 2.1. The processes involved in actual data acquisition are also elaborated to sketch the requirements of overall control. Section 2.2. is devoted to discuss broad view of microcomputer configurations around 8086 (8088). The standard facilities provided by the MASM.COM utility to develop and test the software, either through predefined data sets and manual scrolling or through emulation, form parts of elaboration of Sec.2.3.

2.1. Instrumentation at Low Temperatures

Various methods are adopted to achieve a controlled temperature around the sample. Designs of cryostats based on the principle of evaporating the liquid gases at reduced (increased) partial pressures forms a group[21], fig. 2.1, while use of close cycle refrigerators operating in improved solvey-McMohan cycle, forms the another fig. 2.2[15]. With the cryostatic method temperatures within $\pm$ 4 to 15^{o}K of temperature of liquid at atmospheric pressures are achievable, but the design becomes

complicated if continuously variable temperature, from about 300K to the maximum possible temperature, at the cold station is expected. Cryotips, on the other hand, provide a continuous control of the temperature.

The cryostatic devices are best suited for the measurements of heat-capacity[22,23], Thomson's Coefficient, Thermal conductivity[24], etc., where the adiabatic conditions around the sample are most essential. In practice deviations from the adiabatic conditions are bound to occur and it is mandatory to record the deviation occured during a measurement event, to apply numeric approximations. This evidently demands a calorimetric construction, fig. 2.1, for placing the sample for measurements. Various colorimetric designs for heat-capacity C_p measurements are elaborated by G.K.White[21]. Basic principle behind all these designs is to have a chamber (C) thermally isolated from the liquid at atmospheric temperatures. Within this chamber the liquid gas is poured in a controlled manner and the chamber is simultaneously evacuated at variable rate, using needle valves (V1,V2), where conductance of the line could be precisely varied. This leads to reduced chamber temperatures. Secondly heater within the chamber (C) is used to produce the elavated temperatures. 'Control of heater or needle valves become a key to control the temperature of the inner-chamber'. Further to record adiabatic conditions of the samples various differential thermo-couples, ΔTcs, are installed in the calorimeter. Start and stop measurement sequence are dectated by these differential

temperatures. 'Obviously the measurement setup should accomodate measurement of Δ Tcs as well as has to accomodate a way to decide whether proper equilibrium is achieved or not. After the equilibrium is achieved current/voltage sources are achieved to be triggered and system should proceed in data collection of various induced voltages (Δ Tcs on sample and shield), reference-currents, time-events, etc.' Though the actual parameters to be recorded varies with 'the parameters acquised are required to be stored as arrays for further manipulations'. '**After a measurement sequence is completed the various line fitting, numeric crunching algorithms would be employed on the acquised parameters to calculate the actual magnitude of the property being determined. The results and corresponding temperatures are to be saved (recorded) and process should continue to acquise next data set'.**

Measurement of thermopower Q, electrical conductivity where smaller sample sizes are accomodable[16] and do not have too stringent requirements of adiabatic conditions, cryotips are preferable. Additionally temperatures in the range of liquid He could be achieved with these systems, without having to support gas recovery setup overhead. '**Measurement of Q or σ with this system also has similar requirements as mentioned above. Further it is quite possible to all the refrigerators to cool down the cryotip and Q or σ could be determined by continuously measuring thermo emf and gradient across the sample and then applying interpolation techniques'.**

Another most essential component of the setup is the vacuum systems[25]. As far as control requirements of vacuum setup is concerned, these are listed below :

1) **'Switching between various gauges (transducers) to tap the vacuum level, back-convert the output of gauges to provide magnitude of the pressure levels.**

2) Executed decisions or annunciate the vacuum level for the operators interventions', etc.

The last point to be discussed could be the control environment require to schedulize the measurement sequences. **'These features accomodate controlling the temperature interval between two consecutive measurements, starting and ending temperatures of the desired run, etc.'**

The brief description of activities, not specific to a individual property, and reconcilation with the experience in the field the following H.W. and S.W. requirements for a setup, to be generalised controller for the cryophysics laboratories could be sorted out.

1) Hardware Requirements :

i) Multi-channel ADC port with PGDAs[37]; to preamplify the input for the ADC interface.

ii) Parallel communication ports, with simple and handshaked data transfer mechanisms. These could be used for various applications under programme control, e.g. providing triggering signals and data to current/voltage sources, switching relays of

control or test equipment etc.

iii) Annunciation; may include display + artificial sound interfaces.

2) Soft-Ware Requirements :

i) A interpretable language version allowing input/output of 8 or 16 bit data lengths.

ii) Facility to compare contents of a port and determine direction of flow based on these values.

iii) Provisions of numeric representations and arithmatic operations.

iv) Provision to call preassembled subroutines etc.

To avoid repetition of text a few minor items of requirements are left unlisted but are discussed wherever found relevant.

2.2. The Intel 8086 CPU and Configurations.

The Intel 8086 is a 16 bit multichip central processing unit, a out product of NMOS technology and operates at the clock rates of 8 MHz, through a external clock generator chip 8284. The device optionally operates in single CPU or multi CPU configurations, dictated by pin MN/MX. In the maximum mode, of the microcomputer configuration needs a system bus controller, the 8288 to decode status outputs from the processor into the corresponding control signals[26]. Device being a 40 pin DIP configuration, 16 bits of address and data is outputed in the

multiplexed form. To demultiplex data and latch the address 3 X 8282 (Octal latches) and 2 X 8286 (bi-direction data transcievers)[26] are manufactured by Intel Corporation.

The device has a capability to address upto 1 MB of memory and upto 64K I/O ports. The 1 MB of memory is referred as sixteen segments of 64 KB length, where each segment can start on address, even multiple of 10 H, anywhere in the memory space. The segments for program, data, stack and string destination are managed through four 16 bit registers of the processor, viz. CS, DS, SS and ES. I/O operation occurs in segment 0 only. The system opts register components having 8 bit wide data length and to achieve transfer of LSB and MSB on to the appropriate data paths a output BHE (Bit High Enable) is provided for the memory and I/O decode logic. Remarkable feature of addressing mode offered is that the stack could be accessed as normal data memory, simplifying reentrant programming, and branch instructions with a displacement to point the destination, makes the language best suited for linking relocatable modules.

The CPU is configured out of two asynchronously operating processing unit (1) BIU and (2) EU. BIU fetches data instructions from memory while EU executes the instructions loaded by BIU in a 6 byte wide instruction queue. The time required for instruction fetch becomes effectively zero and increases through put of the system. The block diagram, fig. 2.3, shows configuration the CPU in maximum mode. While accomodating additional processor within

this configuration an elaborate logic of arbitrating the bus requests and grant is desired. This has been achieved through 8289, the bus arbitrar. Having this device is mandatory for the configurations where multiple 8086[28] are to be accomodated in the configuration, while coprocessor (8087, Math-processor) or closely coupled (8089, IO processor) operate on the bus and memory of 8086 itself[28]. These configurations are meant to distribute the control, where trade-off having the control distributed are thoroughly discussed in the text books[29,30]. Block diagram of a multi-CPU (loosely coupled configuration), fig. 2.4, brings out the essential features of the configuration.

2.3. MASM.COM, An Assembler Package.

Various philosophies of software development are available and suitability of any approach is task specific. Out of these approaches modular (modular + top-down or modular + bottom-up) approach allows splitting the problem defination amongst various modules and tested. The tested modules then could be interlinked devicing a program stub. These happened to be too well discussed a matter[31,32] and for the software development of the interpreter the modular approach has been adopted suitably.

While testing the modules developed in the assembly language of 8086 (or 8088) in addition to the debugger available with standard version of MS DOS operating system, utilizes MASM.COM, CREF.COM relieves the system designer from data, stack, program memory management. The facilities offered by the package[33] are highlighted below.

The package allows identifiers to be used to refer variable or fixed data items. Variable data items 1,2,4,8, or 10 bytes wide could be separately identified and are meant for specific purpose, e.g. 10 byte wide data items are intended for maths-coprocessors (8087). Further, multiple choice is offered while inputting operands with instructions.

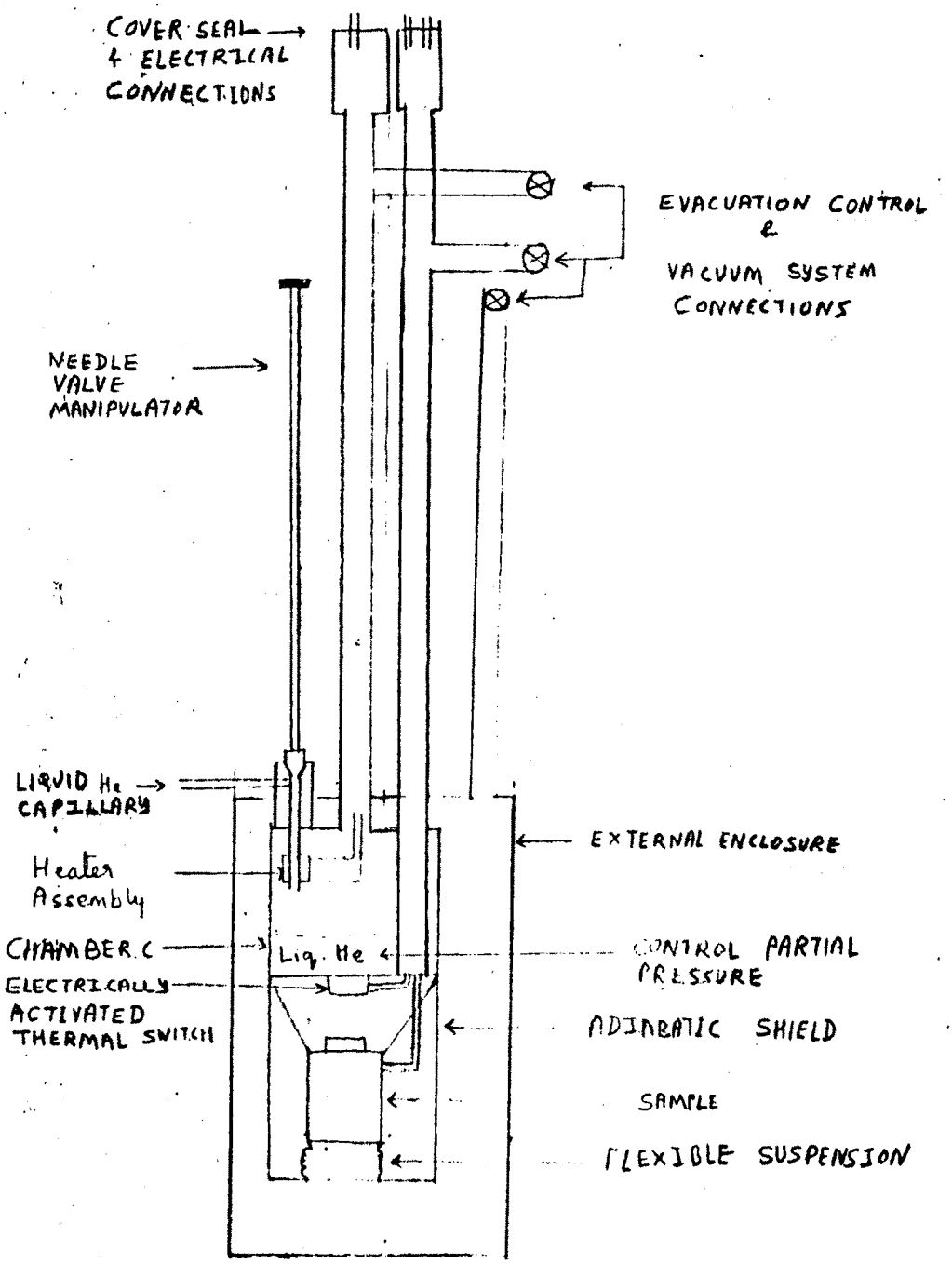
For the management of program flow, labels are allowed with Branch instructions. The labels are prefixed with SHORT, FAR ATTRIBUTES, indicating the jumps within ± 128 bytes, intrasegment direct, intersegment direct, intrasegment indirect and intersegment indirect.

A few more facilities are mentioned below. Segments could be titled and grouped together, data structures could be defined, type of variable identifier could be over ridden etc.

An assembly language file could be assembled through this package and cross references could be optionally echoed to facilitate debugging the object code file generated by the assembler. The codes generated are relocatable and assigning specific segment addresses is left to MS LINK facility available with the MS DOS. However, fixed addressed could be used to specify the desired segment. After the program is loaded into the main memory of the PC, it could be debugged through DEBUG facilities of MS DOS. We conclude this discussion with a mention that not only the object code modules could be tested but .COM or

.BIN could also be generated using EXC2BIN command of MS DOS.

FIG. 2.1. SCHEMATIC OF SPECIFIC-HEAT CRYOSTAT.



THE ASSEMBLY IS DIPPED IN TO LIQUID HE STORAGE (CONTAINER)

FIG 2.2 CLOSE-CYCLE REFRIGERATOR

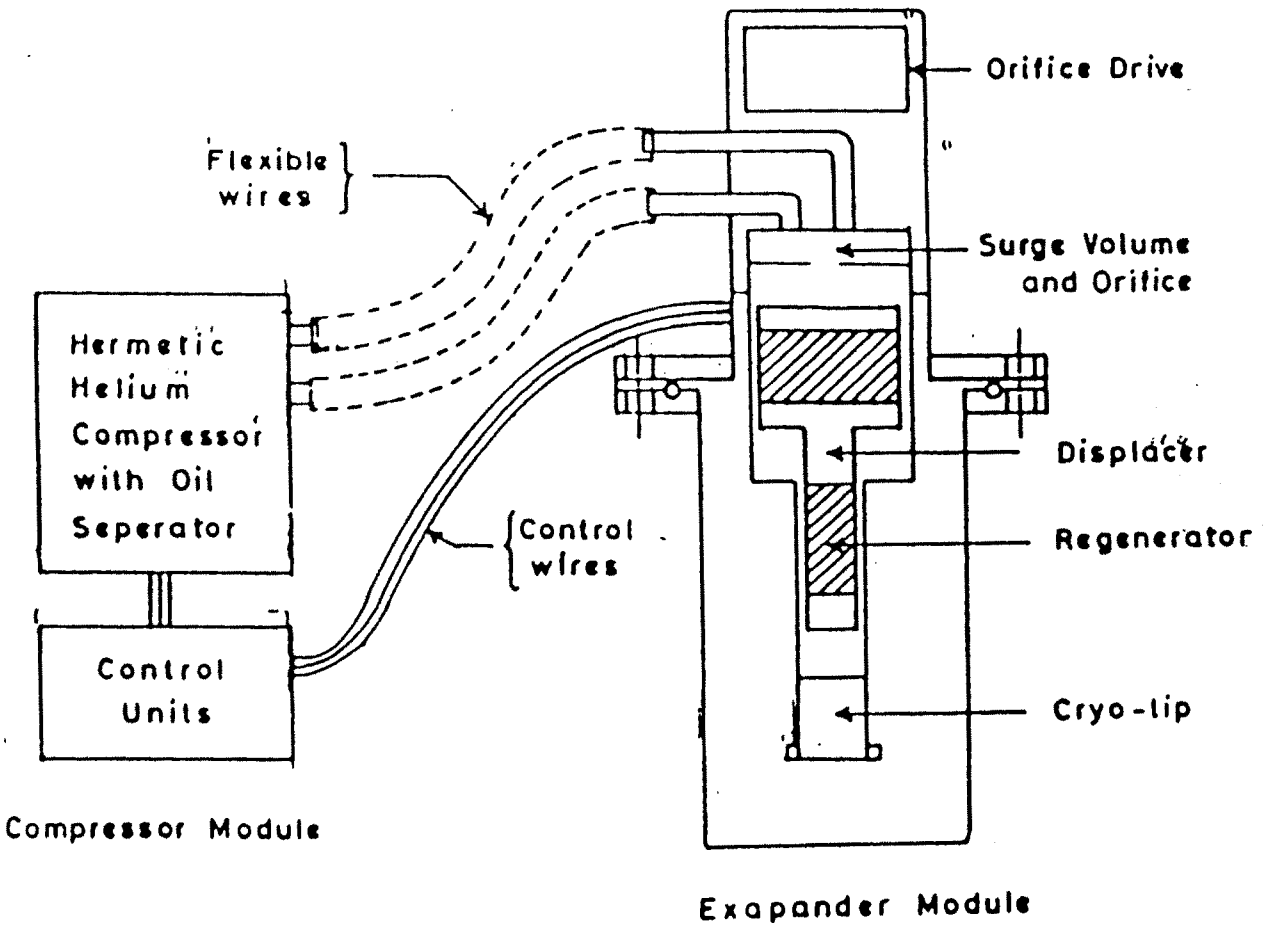


FIG 2.3 THE 8086 IN MAXIMUM MODE

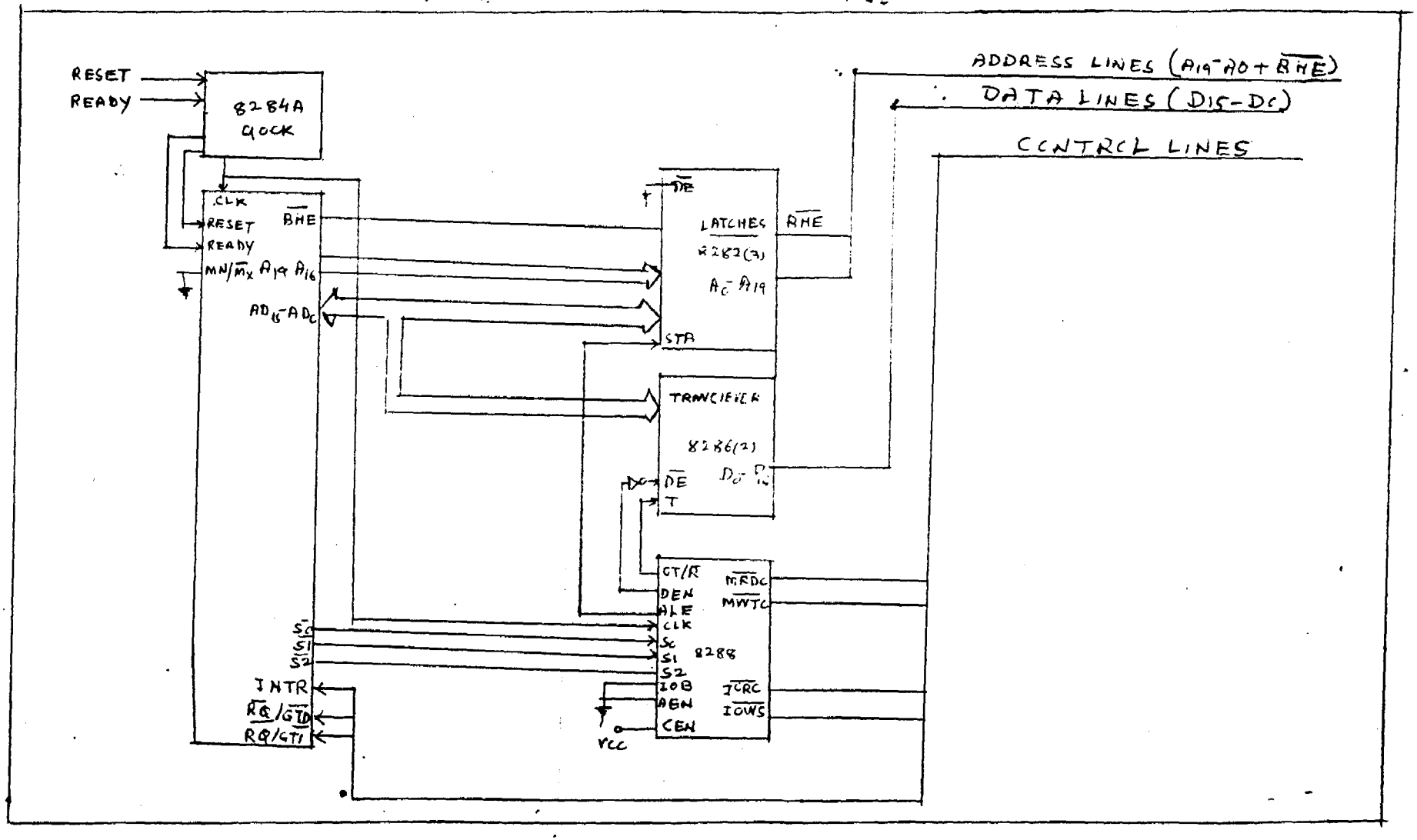


FIG 2.4 LOOSELY COUPLED CONFIGURATION