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RESUMES

Advent in semiconductor technology has endowed us with the digital processors with processing rates as high as 100 Mops of execution cycles per second and the corresponding storage and logic control hardware. These entities diverted the attention of instrumentalists towards thinking in terms of discreet logic to process the information. The high speeds of operation has left the "discreet", a antique prelude.

Recently M/s.Philips Inc. and M/s.Hewlett Packard have introduced their digital storage scopes with the sampling speed of 500MS/sec and bandwidths of 500MHz (2). Commercial viability of these products has inspired us to attempt developing an experience and an expertise in the design of fast digital signal processing and storage systems. The main interest was to develope an involved understanding of design of control hardware/software, where variable sampling speeds are accomodated. Therefore, development of too high sampling rate system was not intended. For the purpose we selected design of a digitising and control interface to a standard 20MHz dual trace analog oscilloscope, as the topic of the project. Further prototyping such a system would definately be of direct practical implementation in the laboratories. 10MS/sec sampling speed and HM203 oscilloscope from M/s.Scientific Instruments, company have been treated as base lines for the design. And the experience, we have received during the course of

project has developed an confidance in us and we think that the project could be extended to result into a signal processing system, specifically for physical instrumentation.

The design is around the flash ADC by RCA, the CA3308, and the sampling clock has 50 nsec pulse width The sampling frequency, varies over a range of 10MHz to 5KHz. The sampling frequency is selected such that 1024 [1K] samples would be acquised per horizontal frame. The time base setting selected dictates the speed of horizontal trace The total width of the horizontal trace has been taken up as 10 cms. The auto mode selection is effective for the time base settings of 50 ms/div or below. Therefore the 0.1 & 0.2 s/div settings have been treated separately as a Slow Mode phenomenon. The maximum sampling frequency limits the continuous sampling for time base settings below 10 us/div. This mode is referred as the Fast Mode. For the time base below 10 μs/div random equivalent sampling technique is employed, treated as Repeatative Mode. The time difference between the trigger and the sampling clock is measured using a modified ECL Vernier Counter. Dependent on the mode of time base settings the samples are acquised and displayed. In the slow mode the acquisition and display is simultaneous. In the fast mode the samples are acquised and displayed as a 1K record. In this mode the triggers are allowed to be anywhere within 1K record. This offers a pre and post trigger view of the signal. The cursors and trigger is managed as a 9th bit with the acquised samples. Separate memory bank are used for the sample and cursor/trigger. In the

repeatative as well as in the save mode no pretrigger view is offered. Owing to these different acquisition/display strategies the address generators and control circuits for Slow, Fast and Repeatative Modes are characteristically different and are separate circuit blocks.

The CA3308 has resolution of 8 bits and the information is distributed over 10 cms of vertical scale. The CRT of the scope is used for signal and information display. The information is meant to annunciate the menu, while setting the interface for a desired sequence of operation.

The CA3308 was not available in the Indian currency. Therefore, the hardware is tested partly and at the level of individual modules The integrated testing is left undone for the want of flash converter mainly and MDS at secondary level.

The complete software development and its testing has compensated the timegap of hardware integrated test. The software accomodates selection of the system in Save, Acquisition+Display and Save-Display Modes. In save mode a sample record of 1K, acquised, is stored for the future reference. While in the save-display mode the information thus saved is displayed on a specified channel. The acquisition+display mode is normal mode of action. The software allows setting of various parameters through pannel [keyboard] or could be selected by default. The software also allows previous operation mode to be selected directly, 'The Enter All Mode'. The mode setting activity of software initializes

the various parameters of action in the reference memory and in the interface latches. This activity is referred as state1 activity within the software. In State1 the action number and flags corresponding to the selected mode of operation are calculated and stored as reference parameters

The action number dictates the action to be executed including selection of proper address generator. The acquisition, display, save, save-display are separate action events. Execution of a particular sequence leads to the desired activity. The action sequencer, state2, sequences the actions properly using the flags set and the interrupt control routines. The sequencing is based on the parsing table developed. Dynamic ' Δ V' and ' Δ T', between cursors set, magnitude calculations and display is also accomodated in this state of software activity. The module as well as the integrated testings of the software developed is performed using the test data sets and a PC/XT interfaced serially to ILCV-2 development system offered by Dynalog Micro System (31).
