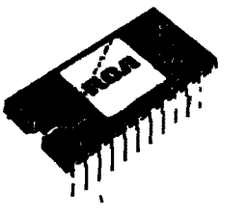
A P P E N D I X



(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:

- *CMOS low power with SOS speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *8-bit latched 3-state output with overflow bit*
- *± ½ LSB accuracy (typ.)*
- *Single supply voltage (4 to 8 V)*
- *2 units in series allow 9-bit output*
- *2 units in parallel allow 30-MHz sampling rate*

The RCA CA3308* is a CMOS 240-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3308 operates over a wide full-scale input-voltage range of 4 volts up to 8 volts with maximum power consumptions as low as 240 mW, depending upon the clock frequency selected. When operated from a 5 volt supply at a clock frequency of 15 MHz, the power consumption of the CA3308 is typically 240 mW.

The intrinsic high conversion rate makes the CA3308 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3308s in series to increase the resolution of the conversion system. A series connection of two CA3308s may be used to produce a 9-bit high-speed converter. Operation of two CA3308s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3308s may be combined with a high-speed 8-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed 15-bit A/D converter.

256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3308.

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

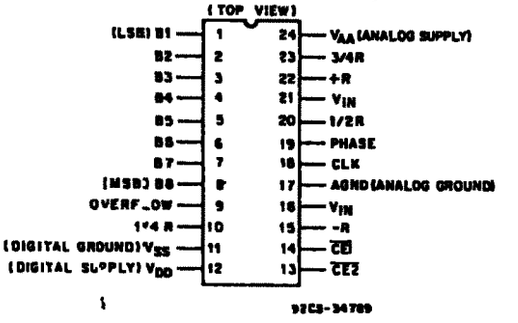
The voltage supply for analog circuitry is termed V_{AA} and AGND. The voltage supply for digital circuitry is termed V_{DD} and V_{SS}.

The CA3308 type is available in a 24-lead dual-in-line ceramic package (D suffix).

* Formerly Developmental Type No. TA11279

Applications:

- *The CA3308 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security/broadcast)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*
- *μP data acquisition systems*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE RANGE (V_{DD} AND V_{AA})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) . . . . . −0.5 to +8 V

INPUT VOLTAGE RANGE
ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

DC INPUT CURRENT
CLK, PH, CE1, CE2, V_{IN} . . . . . ±10 mA

POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A=−40 to 55°C . . . . . 315 mW
FOR T_A=55°C to 85°C . . . . . Derate linearly at 3.3 mW/°C

TEMPERATURE RANGE
OPERATING . . . . . −40 to +85°C
STORAGE . . . . . −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX . . . . . +265°C

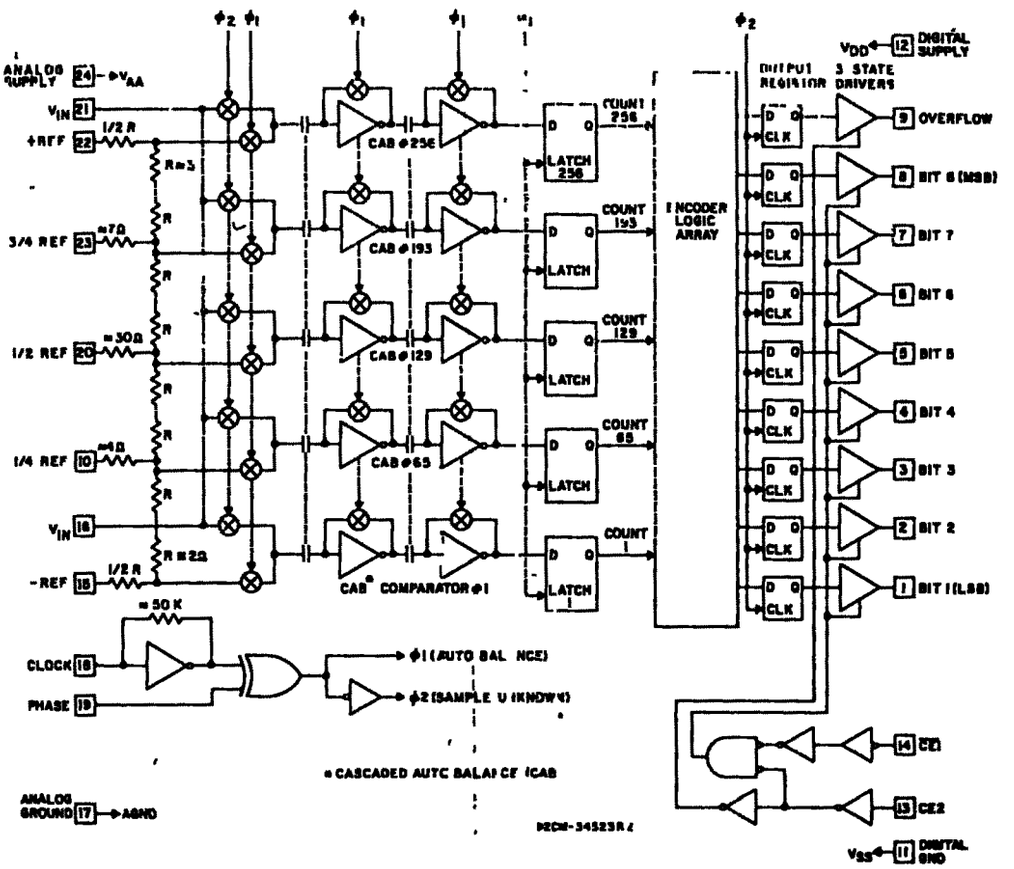


Fig. 1–Block diagram for the CA3308.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V_{AA} = V_{DD}$	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	8	Bits
Linearity Error	V_{DD}=5 V, V_{REF}=6 4 V CLK=15 MHz, gain adjusted	—	—	±1	(CA3308D)
Differential Linearity Error	V_{DD}=5 V_{REF}=6 4 V CLK=15 MHz	—	—	±1	(CA3308D)
Quantizing Error		−½	—	½	LSB
Analog Input	V_{DD}=5 V				
Full Scale Range	CLK=15 MHz	4	—	8	V
Input Capacitance		—	50	—	pF
Input Current	V_{IN}= 6 4 V	—	1000	2000	μA
Maximum Conversion Speed	V_{DD}=5 V	15 M	17 M	—	SPS
Device Current (Excludes I_{REF})	V_{DD}=5 V (CLK=15 MHz)	—	30	—	mA
Ladder Impedance		300	600	900	Ω
Digital Inputs					
Low Voltage		—	—	1 5	V
High Voltage	V_{DD}=5 V	3 5	—	—	V
Input Current (Except Pin 18)		—	±1	—	μA
Digital Outputs					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0 4 V	3 2	10	—	mA
Output High (Source) Current	V_{DD}=5 V, V_O=4 6 V	1 6	−6	—	
Digital Output Delay, t_d	V_{DD}=5 V	—	25	—	ns

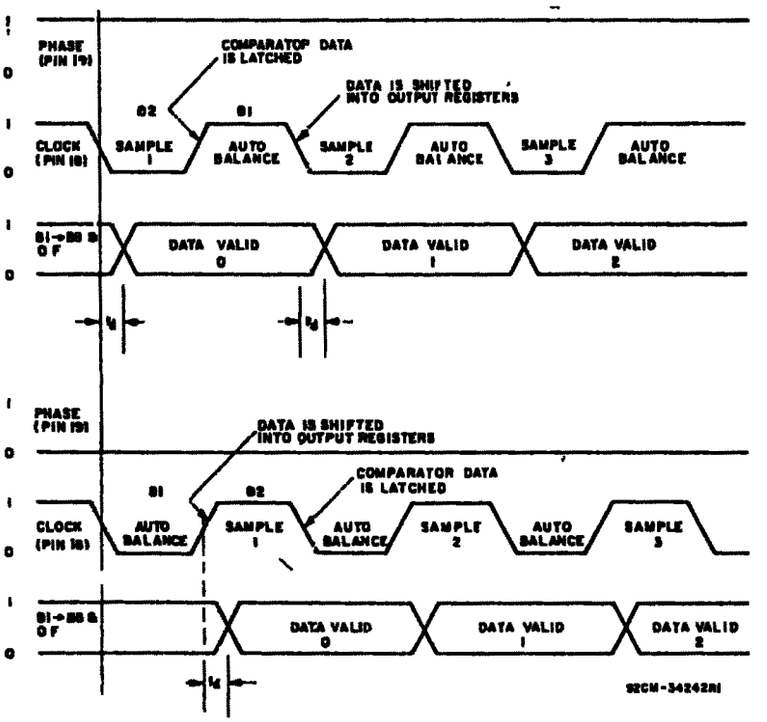


Fig 2-Timing diagram for the CA3308

National Semiconductor

DAC0800, DAC0801, DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1* The reference-to-full-scale current matching of better than ± 1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, potential allow direct interface to all logic families The performance and characteristics of the device are essentially unchanged over the full ±4 5V to ± 18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively

Features

- Fast settling output current — 100 ns
- Full scale error — ± 1 LSB
- Nonlinearity over temperature — ± 0 1%
- Full scale current drift — ± 10 ppm/°C
- High output compliance — −10V to + 18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ± 4 5V to ± 18V
- Low power consumption — 33 mW at ± 5V
- Low cost

Typical Applications

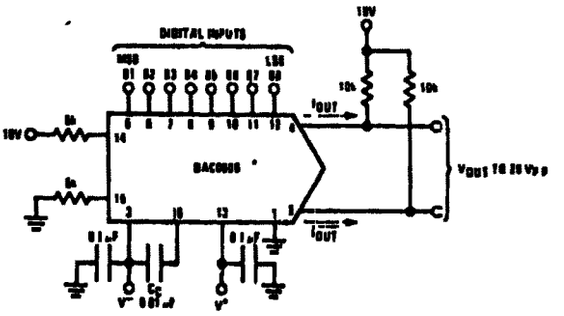
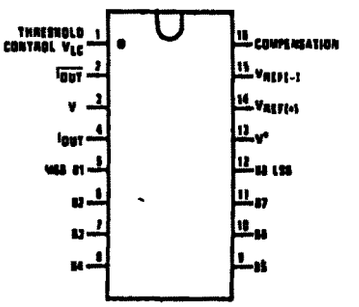


FIGURE 1. ± 20 Vp-p Output Digital-to-Analog Converter

Connection Diagram

Dual-In-Line Package



Top View

TL/H/5686–1

See Ordering Information

Ordering Information

Non Linearity	Temperature Range	Order Numbers*			
		J Package (J16A)		N Package (N16A)	
±0 1% FS	− 55°C ≤ T_A ≤ + 125°C	DAC0802LJ	DAC-08AQ		
±0 1% FS	0°C ≤ T_A ≤ + 70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP
±0 19% FS	− 55°C ≤ T_A ≤ + 125°C	DAC0800LJ	DAC-08Q		
±0 19% FS	0°C ≤ T_A ≤ + 70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP
±0 39% FS	0°C ≤ T_A ≤ + 70°C	DAC0801LCJ	DAC-08CQ	DAC0801LCN	DAC-08CP

*Note Devices may be ordered by using either order number

Absolute Maximum Ratings

Supply Voltage	±18V or 36V
Power Dissipation (Note 1)	500 mW
Reference Input Differential Voltage (V14 to V15)	V⁻ to V⁺
Reference Input Common-Mode Range (V14, V15)	V to V⁺
Reference Input Current	5 mA
Logic Inputs	V⁻ to V⁻ plus 36V
Analog Current Outputs	*Figure 24*
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Temperature (T_A)			
DAC0802L	−55	+125	°C
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0801LC	0	+70	°C
DAC0802LC	0	+70	°C

Electrical Characteristics

(V_S = ±15V, I_{REF} = 2 mA, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter		Conditions	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ½ LSB, All Bits Switched "ON" or "OFF", T_A = 25°C		100	135					100	150	ns
		DAC0800L					100	135				ns
		DAC08C0LC					100	150				ns
t_{PLH}, t_{PHL}	Propagation Delay Each Bit	T_A = 25°C		35	60		35	60		35	60	ns
	All Bits Switched			35	60		35	60		35	60	ns
TC_{IFS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change < ½ LSB, R_{OUT} > 20 MΩ Typ	−10		18	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R14 = 5.000 kΩ R15 = 5.000 kΩ, T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	V^- = −5V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V^- = −8V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels											
V_{IL}	Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			2.0			V
	Logic Input Current	V_{LC} = 0V										
I_{IL}	Logic '0'	−10V ≤ V_{IN} ≤ +0.8V		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	2V ≤ V_{IN} ≤ +18V		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V_S = −15V	−10		18	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S = ±15V	−10		13.5	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	*(Figure 24)*	4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS}$,	Power Supply Sensitivity	4.5V ≤ V^- ≤ 18V		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS}$		−4.5V ≥ V^- ≥ −18V, I_{REF} = 1mA		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
	Power Supply Current	V_S = ±5V, I_{REF} = 1 mA										
I_+				2.3	3.8		2.3	3.8		2.3	3.8	mA
I_-				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
		V_S = 5V, −15V, I_{REF} = 2 mA										
I_+				2.4	3.8		2.4	3.8		2.4	3.8	mA
I_-				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
		V_S = ±15V, I_{REF} = 2 mA										
I_+				2.5	3.8		2.5	3.8		2.5	3.8	mA
I_-				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF} = 1 mA		33	48		33	48		33	48	mW
		5V, 15V, I_{REF} = 2 mA		108	136		108	136		108	136	mW
		±15V, I_{REF} = 2 mA		135	174		135	174		135	174	mW

Note 1: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the dual in line J package must be derated based on a thermal resistance of 100°C/W, junction to ambient; 175°C/W for the molded dual in line N package.

National Semiconductor

MM2147/MM2147L Family 4096 x 1 Static RAMs

General Description

The MM2147 is a 4096 word by 1 bit static random access memory fabricated using N channel silicon gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode.

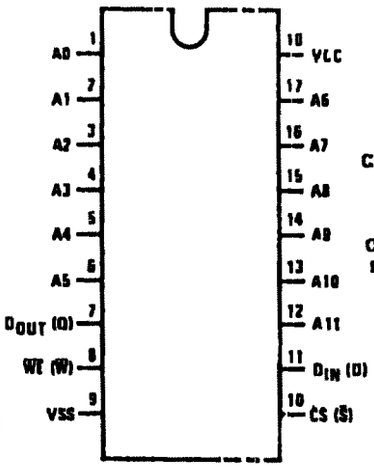
The output is held in a high impedance state during write to simplify common I/O applications.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power down
- High speed—down to 55 ns access time
- TRI STATE® output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18 pin dual in line package

Connection Diagram*

Dual In Line Package

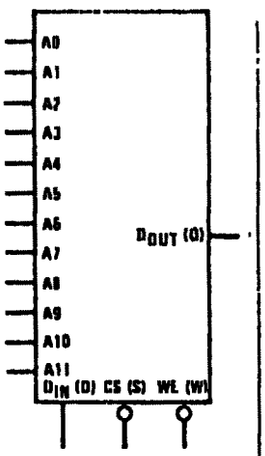


TOP VIEW

Order Number MM2147N 3, MM2147N, MM2147N L or MM2147N 1L
See NS Package N18A

Order Number MM2147J 3, MM2147J, MM2147J L or MM2147J 1L
See NS Package J18A

Logic Symbol*



Pin Names*

A0–A11	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
DIN (D)	Data In
DOUT (O)	Data Out
VCC	Power (+5V)
VSS	Ground

Truth Table*

CS (S)	WE (W)	DIN (D)	DOUT (O)	MODE	POWER
H	X	X	Hi Z	Not Selected	Standby
L	L	H	Hi Z	Write 1	Active
L	L	L	Hi Z	Write 0	Active
L	H	X	DOUT	Read	Active

* The symbols in parentheses are proposed industry standard

Functional Description

Two pins control the operation of the MM2147 Chip select enables write and read operations deselects the device putting it in the low power standby mode and controls TRI STATING of the data output buffer Write enable chooses between READ and WRITE modes and also controls output TRI STATING The truth table details the states produced by combinations of the controls

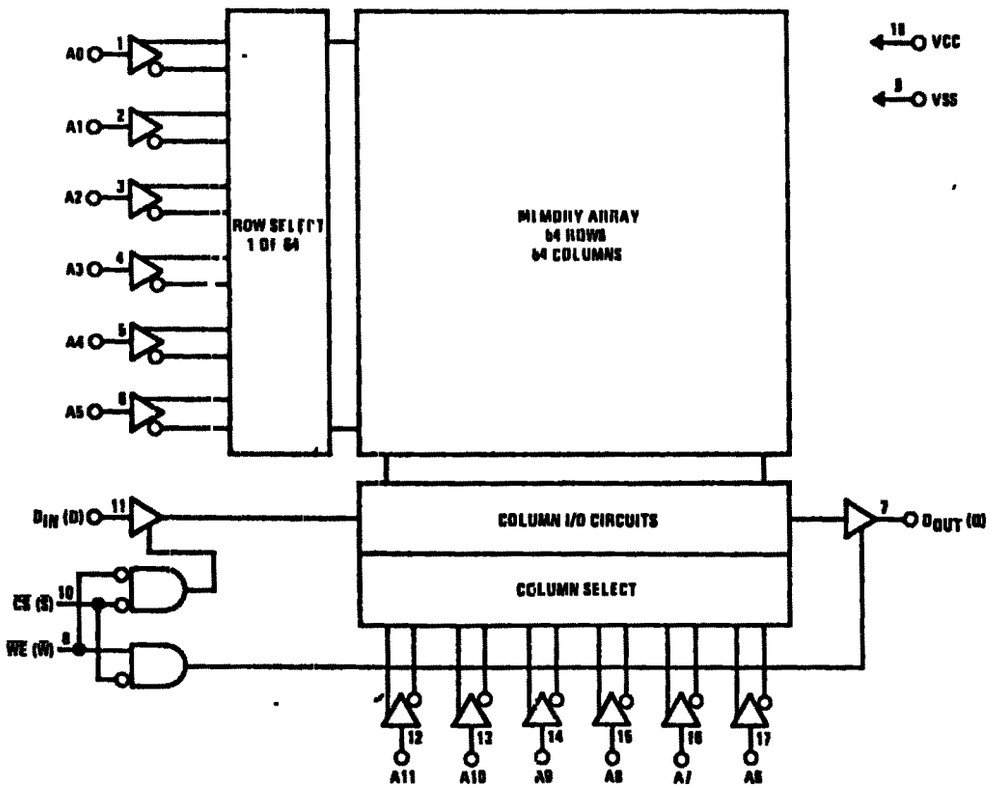
READ cycle timing is shown in the section on Switching Time Waveforms Write enable is kept high Independent of chip select any change in address code causes new data to be fetched and brought to the output buffer Chip select must be low, however, for the output buffer to be enabled and transfer the data to the output pin

Address access time is the time required for an address change to produce new data at the output pin, assuming chip select has enabled the output buffer prior to data arrival Chip select access time is the time required for chip select to enable the output buffer and transfer previously fetched data to the output pin Operation with chip select continuously held low is permissible

WRITE cycle timing is shown in the section on Switching Time Waveforms Writing occurs only during the time both chip select and write enable are low Minimum write pulse width refers to this simultaneous low region Data set up and hold times are measured with respect to whichever control first rises Successive write operations may be performed with chip select continuously held low Write enable then is used to terminate WRITE between address changes Alternatively, write enable may be held low for successive WRITES and chip select used for write interruption between address change In any event, either write enable or chip select (or both) must be high during address transitions to prevent erroneous WRITE

Standby operation allows data to be maintained with approximately 85% less current The device automatically switches to the low power standby mode whenever it is deselected

Block Diagram *



* The symbols in parentheses are proposed industry standard

Absolute Maximum Ratings

Voltage on any Pin Relative to VSS	1 5V to +7V
Storage Temperature Range	65°C to +150°C
Power Dissipation	1 2W
DC Output Current	20 mA
Bias Temperature Range	10°C to +85°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (VCC)	4 5	5.5	V
Ambient Temperature (TA)	0	+70	°C

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MM2147 3		MM2147		MM2147L MM2147L 1		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
VIH	Logical '1' Input Voltage		2 0	6 0	2 0	6 0	2 0	6 0	V
VIL	Logical '0' Input Voltage		1 0	0 8	1 0	0 8	1 0	0 8	V
VOH	Logical '1' Output Voltage	IOH = 1 0 mA	2 4		2 4		2 4		V
VOL	Logical '0' Output Voltage	IOL = 8 0 mA		0 4		0 4		0 4	V
ILI	Input Load Current	VIN = 0 to 5 5V, VCC = Max		10		10		10	µA
ILO	Output Leakage Current	VOUT = 4 5V to Gnd, $\overline{CS}$ = VIH, VCC = Max		50		50		50	µA
ICC1	Power Supply Current	VCC = Max $\overline{CS}$ = VIL, Outputs Open, TA = 25°C		170		160		135	mA
ICC2	Power Supply Current	VCC = Max $\overline{CS}$ = VIL Outputs Open TA = 0°C		180		180		140	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		30		20		10	mA
IPO	Peak Power ON Current (Note 2)	VCC = Gnd to VCC Min, $\overline{CS}$ = Lower of VCC or VIH (MIN)		70		50		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
CIN	Input Capacitance	All Inputs VIN = 0V		5	pF
COUT	Output Capacitance	VOUT = 0V		6	pF

AC Test Conditions (Note 4)

Input Pulse Levels	Gnd to 3 5V
Input Rise and Fall Times	≤ 10 ns
Input and Output Timing Reference Levels	1 5V
Output Load	See *Figure 1*

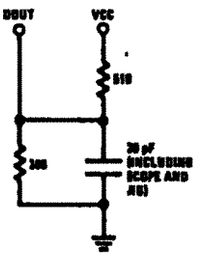


FIGURE 1. Output Load

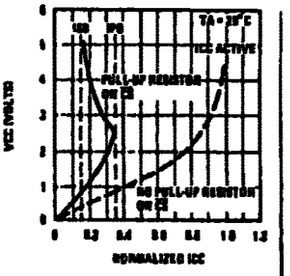


FIGURE 2. Power On Current

Note 1: Guaranteed with transverse air flow greater than 400 linear feet per minute

Note 2: A pull-up resistor to VCC on the chip select input is required to keep the device deselected or power on current approaches ICC active (see *Figure 2*)

Note 3: This parameter is guaranteed by periodic testing

Note 4: This device requires a 500 µs time delay after VCC reaches the specified minimum limit to ensure proper operation after power on This allows the internally generated substrate bias to reach its functional level

Read Cycle AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10%

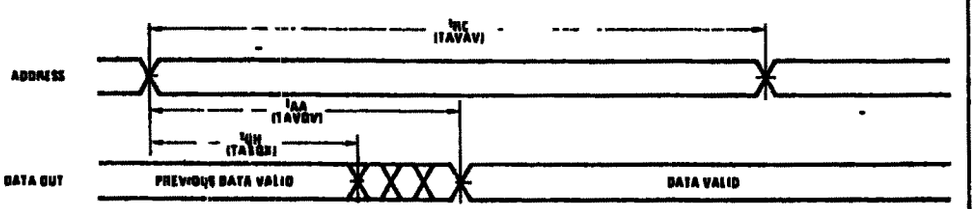
SYMBOL		PARAMETER	MM2147-3		MM2147 MM2147L		MM2147L-1		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	t_{AVAV}	Read Cycle Time	55		70		90		ns
t_{AA}	t_{AVQV}	Address Access Time		55		70		90	ns
t_{ACS1}	t_{SLQV1}	Chip Select Access Time (Note 5)		55		70		90	ns
t_{ACS2}	t_{SLQV2}	Chip Select Access Time (Note 6)		65		80		105	ns
t_{OH}	t_{AXQX}	Output Hold from Address Change	5		5		5		ns
t_{LZ}	t_{SLQX}	Chip Selection to Output Active	0		10		10		ns
t_{HZ}	t_{SHQZ}	Chip Deselection to Output TRI-STATE	0	40	0	40	0	50	ns
t_{PU}	t_{SLICCH}	Chip Selection to Power Up	0		0		0		ns
t_{PD}	t_{SLICCL}	Chip Deselection to Power Down		30		30		35	ns

Note 5 Chip deselected for greater than 55 ns prior to selection

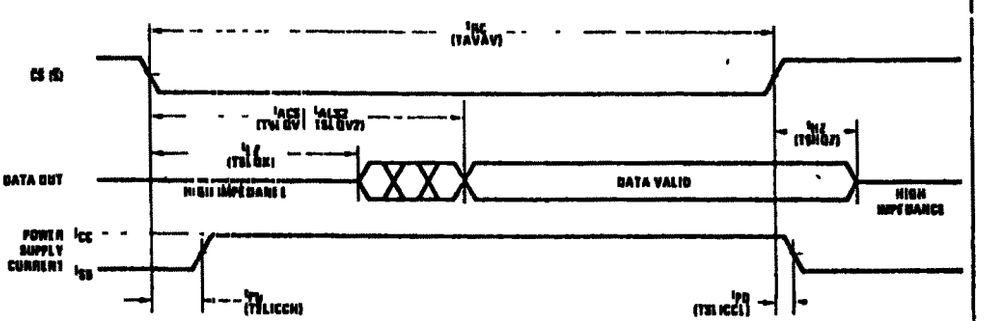
Note 6 Chip deselected for a finite time that is less than 55 ns prior to selection

Read Cycle Waveforms*

Read Cycle No. 1 (Continuously Selected)



Read Cycle No. 2 (Chip Select Switched)



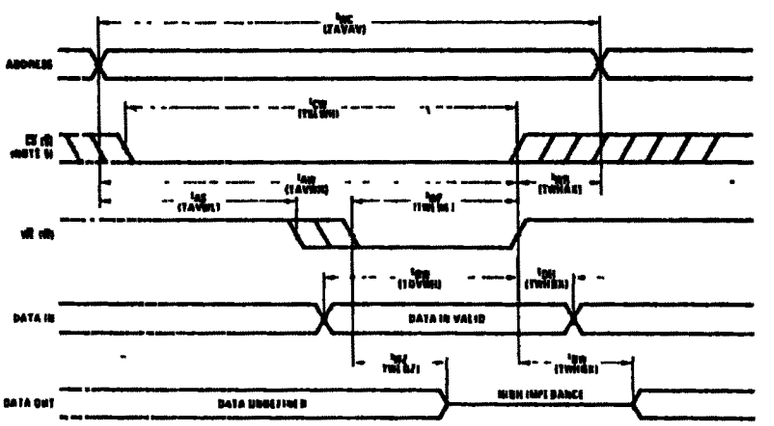
* The symbols in parentheses are proposed industry standard

Write Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

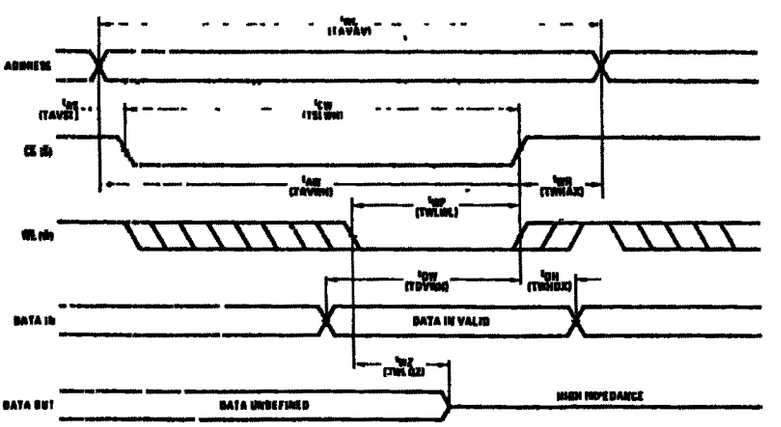
SYMBOL		PARAMETER	MM2147-1		MM2147, MM2147L		MM2147L-1		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	t_{AVAV}	Write Cycle Time	55		70		80		ns
t_{CW}	t_{ELWH}	Chip Selection to End of Write	45		55		60		ns
t_{AW}	t_{AVWH}	Address Valid to End of Write	45		55		60		ns
t_{AS}	t_{AVWL} t_{AVEL}	Address Setup Time	0		0		0		ns
t_{WP}	t_{WLWH}	Write Pulse Width	35		40		60		ns
t_{WR}	t_{WHAX}	Write Recovery Time	10		15		20		ns
t_{DW}	t_{DVWH}	Data Valid to End of Write	25		30		35		ns
t_{DH}	t_{WHDX}	Data Hold Time	10		10		10		ns
t_{WZ}	t_{WLQZ}	Write Enabled to Output in Hi-Z	0	30	0	35	0	40	ns
t_{OW}	t_{WHQX}	Output Active from End of Write	0		0		0		ns

Write Cycle Waveforms* (Note 7)

Write Cycle No. 1 ($\overline{WE}$ Controlled)



Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note 7: A write occurs during the coincidental low of $\overline{CS}$ and $\overline{WE}$. The output remains TRI-STATE® if $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during address transitions.

* The symbols in parentheses are proposed industry standard

National Semiconductor

NMOS RAMs
PREVIEW

NMC2148/NMC2148L 1024 × 4 Static RAM

General Description

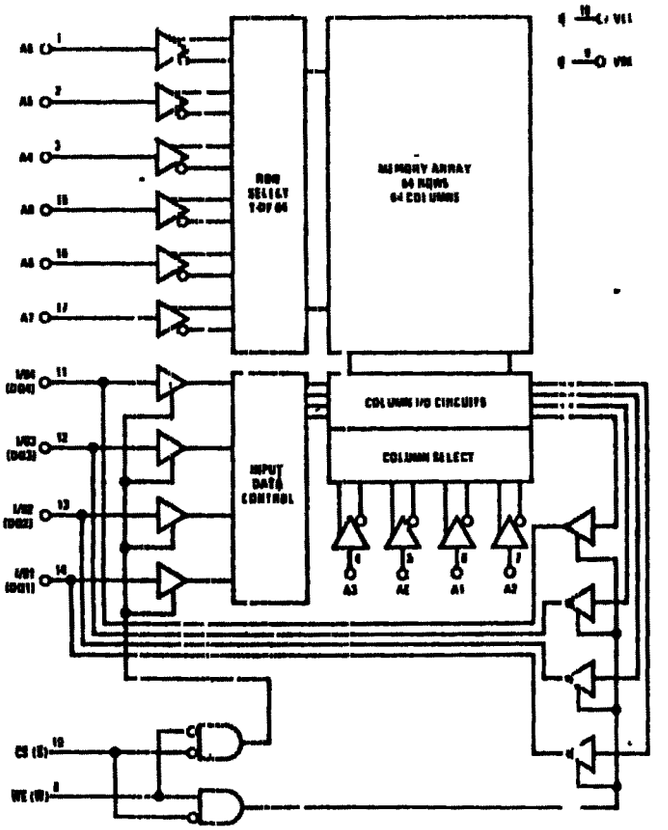
The NMC2148 is a 1024 word by 4-bit static random access memory fabricated using N-channel silicon gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high. Common input/output pins are provided.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power down
- High speed: down to 55 ns access time
- TRI-STATE® output for bus interface
- Common Data I/O pins
- Single +5V supply
- Standard 18 pin dual in-line package

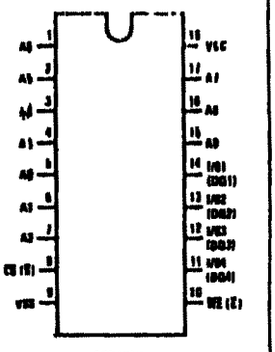
Block Diagram*



*The symbols in parentheses are proposed industry standard

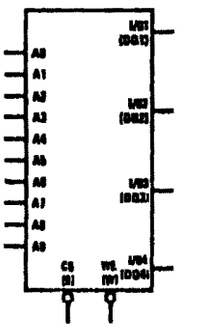
Connection Diagram*

Dual In-Line Package



TOP VIEW

Logic Symbol*



Pin Names*	
A0-A9	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
I/O1-I/O4 (DQ1-DQ4)	Data Input/Output
VCC*	Power (+5V)
VSS	Ground

ECL10 000

These specifications cover the electrical characteristics of the ECL10 000 unless otherwise specified in the individual device data sheet.

RATINGS: see chapter "MAXIMUM RATINGS"

DC CHARACTERISTICS at V_{CC} = ground, V_{EE} = −5,2 V

Each ECL circuit has been designed to meet the d.c. specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow of 2,5 m/s is maintained. Test values are given in the table and defined in the figure.

Test parameters:

	temperature °C			unit
	−30	+25	+85	
V_{IHmax}	−890	−810	−700	mV
V_{IHmin}	−1205	−1105	−1035	mV
V_{ILmax}	−1500	−1475	−1440	mV
V_{ILmin}	−1890	−1850	−1825	mV

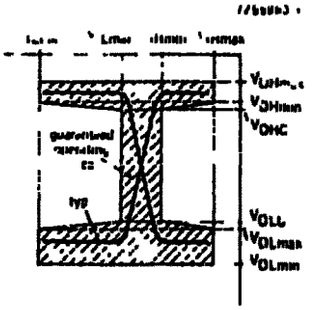


Fig. 1 Transfer characteristics.

AC CHARACTERISTICS

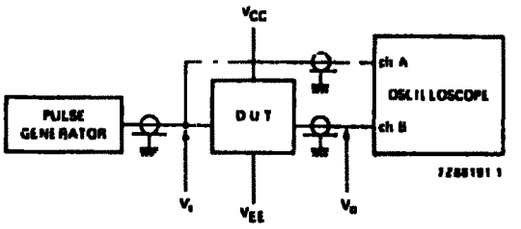


Fig. 2 Switching times test circuit $V_{CC1} = V_{CC2} = +2,0$ V, $V_{EE} = -3,2$ V.

input pulse: $t_{TLH} = t_{THL} = 2,0 \pm 0,2$ ns (between 20 and 80%); $V_{IH} = +1,1$ V; $V_{IL} = +0,3$ V.

Test table V_{CC} = 0 V (ground); V_{EE} = −5,2 V; R_L = 50 Ω to −2 V.

characteristic	symbol	temperature (°C)			unit	remarks
		−30	+ 25	+ 85		
Output voltage HIGH	V_{OHmax}	−890	−810	−700	mV	
	V_{OHmin}	−1060	−960	−890	mV	
Output threshold voltage HIH	V_{OHC}	−1080	−980	−910	mV	
Output threshold voltage LOW	V_{OLC}	−1655	−1630	−1595	mV	
Output voltage LOW	V_{OLmax}	−1675	−1650	−1615	mV	
	V_{OLmin}	−1890	−1850	−1825	mV	

Notes

1 Input resistance is positive at any frequency.

2 Non specified input pins should be connected to V_{ILmin} or left open.

3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal lenght.

4 Input impedance of the oscilloscope is 50 Ω.

5 The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper test.

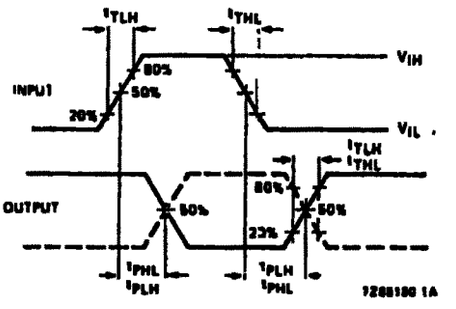


Fig. 3 Propagation delay and transition times waveforms

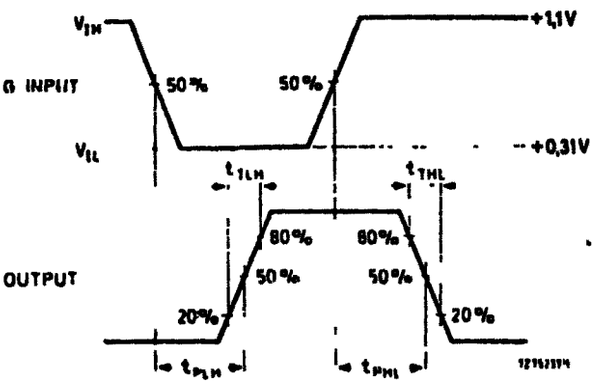


Fig 5 Switching times testing waveforms

QUADRUPLE OR/NOR GATE

The 10101 is a quadruple 2 input OR/NOR gate with one input from each gate common to pin 12. Unused inputs can be left open due to integrated pull down resistors, which avoids the need for a voltage supply.

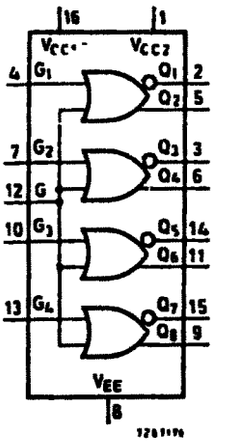


Fig 1 Logic diagram

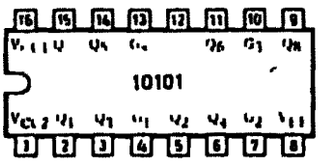


Fig 2 Pin designation

$V_{CC1} = V_{CC2} = 0$ V (ground),
$V_{EE} = -5,2$ V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2	V
Operating ambient temperature range	T_{amb}		−30 to + 85	°C
Average propagation delay	t_{pd}	typ	2,0	ns
Output voltage				
HIGH state	V_{OH}	nom	-880	mV
LOW state	V_{OL}	nom	-1720	mV
Power consumption per package (no load)	P_D	typ	100	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package outlines)

10101N plastic 16-lead dual in-line (SOT 38)
10101F ceramic 16-lead dual in line (SOT-74)

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	conditions
Supply current	I_{EEmax}	8	29	26	26	mA	
Input current LOW	$I_{IL\,min}$	4*	0,5	0,5	0,3	μA	see 'How to test section'
Input current HIGH	I_{IHmax}	12*	850	535	265	μA	
		other inputs	425	265	265	μA	

* Individually test each input applying the above mentioned conditions

Output voltage HIGH	V_{OH}	min	−1 060	960	− 890	mV	V_{ILmin} on inputs
		typ		880		mV	for invert outputs
		max	890	− 810	− 700	mV	V_{IHmax} on inputs for direct outputs
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{IHmax} on inputs
		typ		−1 720		mV	for invert outputs
		max	−1 675	−1 650	−1 615	mV	V_{ILmin} on inputs for direct outputs
Output threshold voltage HIGH	V_{OHC}	min	−1060	− 980	− 910	mV	V_{ILC} on one input for invert ouputs; V_{IHC} on one input for direct outputs
Output threshold voltage LOW	V_{OLC}	max	−1 655	1 630	1 595	mV	One input at V_{ILC} or V_{IHC}

A C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2 0 V, V_{EE} = −3.2 V, R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	conditions
Propagation delay times	t_{PLH}/ t_{PHL}	min	1,0	1,0	1,0	ns	
		typ.		2,0		ns	50% to 50%
		max	3,1	2,9	3,3	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ		2,0		ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For switching times test circuit and waveform see Family Specifications

QUADRUPLE NOR GATE

The 10102 is a quadruple 2-input NOR gate

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply

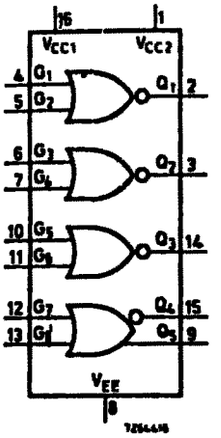


Fig 1 Logic diagram

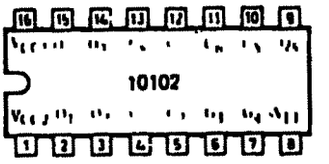


Fig 2 Pin designation

$V_{CC1} = V_{CC2} = 0$ V (ground),
$V_{EE} = -5,2$ V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom	−880 mV
LOW state	V_{OL}	nom	−1720 mV
Power consumption per package (no load)	P_D	typ	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

10102N: plastic 16-lead dual in-line (SOT 38)
10102F: ceramic 16-lead dual in-line (SOT-74)

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C) −30	+25	+85	unit	conditions
Supply current	I_{EEmax}	8	29	26	29	mA	
Input current LOW	I_{ILmin}	4 *	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	425	265	265	μA	

*Individually test each input applying the same above mentioned conditions

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{ILmin} on inputs
		typ		− 880		mV	for invert outputs
		max	− 890	− 810	− 700	mV	V_{IHmax} on inputs 12,13 for output 9
Output voltage LOW	V_{OL}	min	−1 890	−1 850	−1 825	mV	V_{IHmax} on inputs
		typ		−1 720		mV	for invert outputs
		max	−1 675	−1 650	−1 615	mV	V_{ILmin} on inputs 12;13 for output 9
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{ILC} on one input for invert outputs; V_{IHC} on input 12 or 13 for input 9
Output threshold voltage LOW	V_{OLC}	max	−1 655	−1 630	−1 595	mV	one input at V_{ILC} or V_{IHC}

A C CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C) −30	+25	+85	unit	conditions
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	50% to 50%
		typ.		2,0		ns	
		max.	3,1	2,9	3,3	ns	
transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		typ.		2,0		ns	
		max.	3,6	3,3	3,7	ns	

For switching times test circuit and waveform see Family Specifications.

TTL-TO-ECL TRANSLATOR

The 10124 is a quadruple TTL-to-ECL translator with individual and common TTL compatible inputs on each gate. When the common input is in the LOW state, all ECL direct outputs are in a LOW state and inverting outputs in a HIGH state.

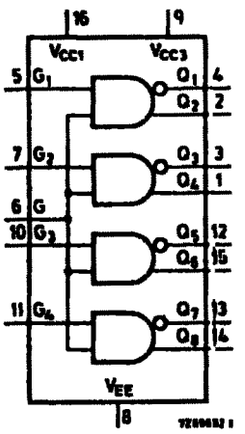


Fig 1 Logic diagram.

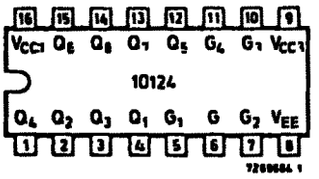


Fig 2 Pin designation.

V_{CC1} = 0 V (ground).
V_{CC3} = +5 V.
V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltages	V_{EE}		−5,2 V
	V_{CC}		+5,0 V
	V_{CCmax}		+7,0 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ	3,5 ns
Output voltage			
HIGH state	V_{OH}	nom	−880 mV
LOW state	V_{OL}	nom	1720 mV
Power consumption per package (no load)	P_D	typ	380 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10124N: plastic 16-lead dual in-line (SOT-38).
10124F: ceramic 16-lead dual in-line (SOT-74).

D.C. CHARACTERISTICS

V_{CC1} = ground; V_{CC3} = +5.0 V; V_{EE} = −5.2 V

	symbol	T_{amb} (°C)			unit	conditions
		−30	+25	+85		
Input voltage						
HIGH max	V_{IHmax}	4,0	4,0	4,0	V	
HIGH min	V_{IHmin}	2.0	1,8	1,8	V	
Input voltage						
LOW min	V_{ILmin}	0,4	0,4	0,4	V	
LOW max	V_{ILmax}	1,1	1,1	0,8	V	
Reverse voltage	V_R	2,4	2,4	2,4	V	
	V_{RH}	4,0	4,0	4,0	V	
Supply current	I_{EEmax}	72	66	72	mA	
	I_{CCHmax}	16	16	18	mA	$V_I = V_{RH}$ (all inputs)
	I_{CCLmax}	25	25	25	mA	
Reverse current						
Strobe input	I_{SR}	200	200	200	μA	$V_I = V_R$ (strobe) V_{ILmin} single inputs
single inputs	I_{IR}	50	50	50	μA	$V_I = V_{ILmin}$ (strobe) V_R (P U T)
Forward current						
strobe input	I_{SF}	−12 8	−12.8	−12.8	mA	$V_I = V_{ILmin}$ (strobe) V_R (single inputs)
single inputs	I_{IF}	− 3 2	− 3 2	− 3 2	mA	$V_I = V_R$ (strobe) V_{ILmin} (P.U T)
Input breakdown voltage	$V_{I(BR)min}$	5,5	5,5	5,5	V	I_I strobe = 1 mA $V_I = V_{ILmin}$ while testing single inputs
Input clamping voltage						
I_5, I_7, I_{10}, I_{11}	$V_{I(Cl)max}$	− 1,5	− 1,5	− 1,5	V	test one input at a time I_I = −10 mA
I_6	$V_{I(CL)max}$	− 1,5	− 1,5	− 1,5	V	I_I = −20 mA

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Output voltage HIGH	V_{OH}	min	−1 060	− 960	−890	mV	For outputs 1,2,14,15: pins 5,6,7,10,11 at V_{IHmax} For outputs 3,4,12,13: pins 5,6,7,10,11 at V_{ILmin}
		typ		− 880		mV	
		max	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min	-1 890	-1 850	-1 825	mV	For outputs 1,2,14,15: pins 5,6,7,10,11 at V_{ILmin} For outputs 1,2,14,15: pins 5,6,7,10,11 at V_{IHmax}
		typ		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 060	− 980	− 910	mV	For outputs 1,2,14,15: one input at V_{IHC} (1); other inputs at V_{IH} For outputs 3,4,12,13: one input at V_{ILC}; other inputs at V_{IH} (1)
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For outputs 1,2,14,15: one input at V_{ILC} (1); other inputs at V_{IHmax} For outputs 3,4,12,13: one input at V_{IHC}; other inputs at V_{IHmax}

V_{CC} must be applied before V_{EE} or simultaneously.

(1) per translator.

A C CHARACTERISTICS

V_{CC1} = 2 0 V, V_{CC3} = 7.0 V; V_{EE} = 3 2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	V_I (+1.5 V) to V_O (50%)
		typ.		3,5		ns	
		max.	6,8	6,0	6,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min	1,0	1,1	1,1	ns	20% to 80%
		max.	4,2	3,9	4,3	ns	

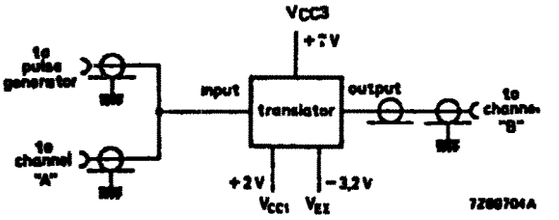


Fig. 6 Switching times test circuit

Input pulse: $t_{TLH} = t_{THL} = 5{,}5$ ns (10 to 90%)

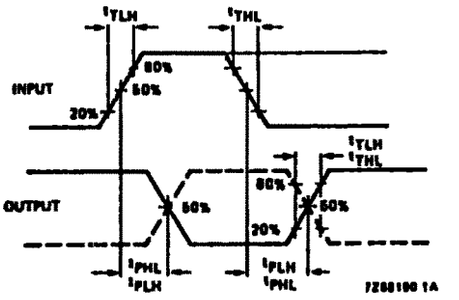


Fig 8 Switching times waveforms. Input voltage at 50%1,5 V

ECL-to-TTL TRANSLATOR

The 10125 is a quadruple ECL-toTTL translator for interfacing data between two different logic systems. It provides also a separate reference voltage (V_{BB}) to be used in case of single ended input biasing. Input and output levels are respectively ECL 10 000 and TTL Schottky. With translated emitter follower inputs and an active current source, it features a common mode rejection peak voltage of ± 1 V.

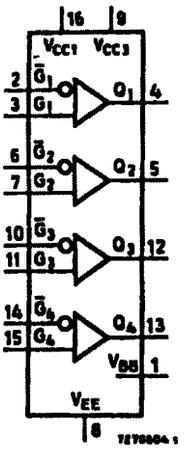


Fig 1 Logic diagram.

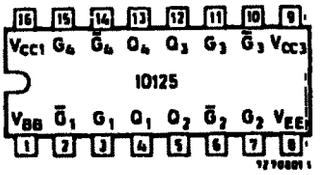


Fig 2 Pin designation

V_{CC1} = 0 V (ground).
V_{CC3} = + 5 V.
V_{EE} = −5,2 V

QUICK REFERENCE DATA

Supply voltages	V_{EE}		−5,2 V
	V_{CC2}		+5,0 V
	V_{CCmax}		+7,0 V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ	4,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	3,5 V
LOW state	V_{OL}	nom.	0,3 V
Power consumption per package (no load)	P_D	typ.	380 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10125N: plastic 16-lead dual in-line (SOT 38).
10125F: ceramic 16-lead dual in-line (SOT-74)

D.C. CHARACTERISTICS

V_{CCL} 0 V (ground), V_{EE} = −5.2 V, V_{CC3} = +5 V

	symbol	Tamb (°C)			unit	conditions
		−30	+25	+85		
Supply current	I_{CCHmax}	52	52	52	mA	For pins 3,7,11,15 $V_I = V_{BB}$ For pins 2,6,10,14 $V_I = V_{IHmax}$
	I_{CCLmax}	39	39	39	mA	For pins 3,7,11,15 $V_I = V_{BB}$ For pins 2,6,10,14 $V_I = V_{ILmin}$
Supply current	I_{EEmax}	44	40	44	mA	For pins 3,7,11,15 $V_I = V_{BB}$ For pins 2,6,10,14 $V_I = V_{ILmin}$
Input current	I_{IHmax}	180	115	115	μA	$V_{I1} = V_{IHmax}$ $V_{I2} = V_{IHA}$ (Fig. 4)
	I_{CBOmax}	1,5	1,0	1,0	μA	$V_{I1} = V_{EE}$ $V_{I2} = V_{EE}$ (Fig. 4)
Short-circuit output current	I_{OS} min	40	40	40	mA	For pins 3,7,11,15 $V_I = V_{BB}$
	I_{OS} max	100	100	100	mA	For pins 2,6,10,14 $V_I = V_{ILmin}$ Connect outputs to ground, one at a time
Output voltage HIGH min	V_{OHmin}	2,5	2,5	2,5	V	Pins 2,6,10,14 $V_I = V_{ILmin}$ (1) Pins 3,7,11,15 $V_I = V_{IHmax}$
LOW max	V_{OLmax}	0,5	0,5	0,5	V	Pins 2,6,10,14 $V_I = V_{IHmax}$ Pins 3,7,11,15 (2) $V_I = V_{ILmin}$
Threshold voltage HIGH	V_{OHC}	2,5	2,5	2,5	V	Pins 2,6,10,14 $V_I = V_{ILmax}$ (one input a time) (1) Pins 3,7,11,15 $V_I = V_{BB}$
Threshold voltage LOW	V_{OLC}	0,5	0,5	0,5	V	Pins 2, 6, 10, 14 $V_I = V_{IHmin}$ (2) (one input at a time) Pins 3, 7, 11, 15 $V_I = V_{BB}$
Indeterminate input protection	$V_{OLS1max}$	0,5	0,5	0,5	V	All inputs at V_{EE} Test one gate at a time (2)
	$V_{OLS2max}$	0,5	0,5	0,5	V	All inputs open (2)

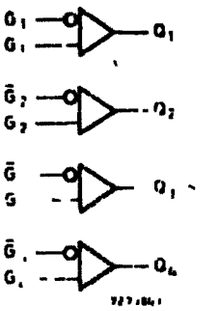
	symbol	T_{amb} (°C)			unit	conditions
		−30	+25	+85		
Reference voltage	V_{BB} min	−1 280	−1 230	−1 150	mV	See general specification "How we test"
	V_{BB} max	−1 420	−1 350	−1 295	mV	
Common mode rejection tests	V_{OH} min	2,5	2,5	2,5	V	V_I = V_{IHH} or V_{IHL} to one input of each gate under test (1) and V_I = V_{ILH} or V_{ILL} respectively to the other input of each gate (2)
	V_{OL} max	0,5	0,5	0,5	V	

(1) Output current is −2,0 mA
(2) Output current is +20,0 mA

A.C CHARACTERISTICS

V_{CC1} = 0 (ground); V_{EE} = −5,2 V; V_{CC3} = 5,0 V

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/t_{PHL}	min	1,0	1,0	1,0	ns	VI 50% to V_O = 1.5 V for single-ended input testing, one input from each gate must be tied to V_{BB} (pin 1)
		typ.		4,5		ns	
		max.	6,0	6,0	6,0	ns	
Transition times rise and fall	t_{TLH}/t_{THL}	max.	3,3	3,3	3,3	ns	(+1 V to +2 V)



$C_1 = G_1$
$C_2 = G_2$
$C_3 = G_3$
$C_4 = G_4$

Positive logic
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig 3 Logic function

TEST PARAMETERS

To meet V_{OH} and V_{OL} specifications $V_i = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL} respectively to the other input of each gate

symbol	T_{amb} (°C)			unit	conditions
	−30	+25	+85		
V_{IHH}	+ 110	+ 190	+ 300	mV	shifted +1 V
V_{IHmax}	− 890	− 810	− 700	mV	
V_{IHL}	−1 890	−1 810	−1 700	mV	shifted −1 V
V_{IHmin}	−1 205	−1 105	−1 035	mV	
V_{ILmax}	−1 500	−1 475	−1 440	mV	
V_{ILH}	− 890	− 850	− 825	mV	shifted +1 V
V_{ILmin}	−1 890	−1 850	−1 825	mV	
V_{ILL}	−2 990	−2 850	−2 825	mV	shifted −1 V

V_{IHH} = V_{IHmax} shifted positive one volt for CMR tests (*)
V_{IHL} = V_{IHmax} shifted negative one volt for CMR tests (*)
V_{ILH} = V_{ILmin} shifted positive one volt for CMR tests (*)
V_{ILL} = V_{ILmin} shifted negative one volt for CMR tests (*)

(*) CMR = Common Mode Rejection

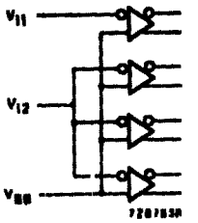


Fig. 4 Input current test circuit
for I_{IH} $V_{I1} = V_{I2} = V_{IH\ max}$
for I_{CBO} $V_{I1} = V_{I2} = V_{EE}$

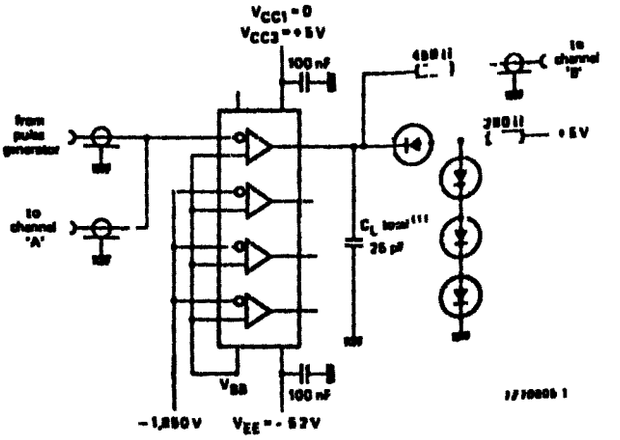


Fig. 5 Switching times test circuit

(1) Including jig and stray capacitance

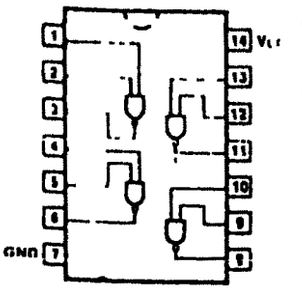
Input pulse: $t_{THL} = t_{TLH} = 2$ ns (20 to 80%)

One input from each gate must be tied to V_{EE} (Pin 1) during testing

54/7400
54H/74H00
54S/74S00
54LS/74LS00

QUAD 2-INPUT NAND GATE

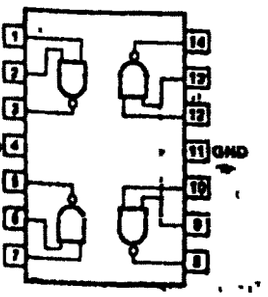
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7400PC, 74H00PC 74LS00PC, 74S00PC		9A
Ceramic DIP (D)	A	7400DC, 74H00DC 74LS00DC, 74S00DC	5400DM, 54H00DM 54LS00DM, 54S00DM	6A
Flatpak (F)	A	74LS00FC, 74S00FC	54LS00FM, 54S00FM	3I
	B	7400FC, 74H00FC	5400FM, 54H00FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

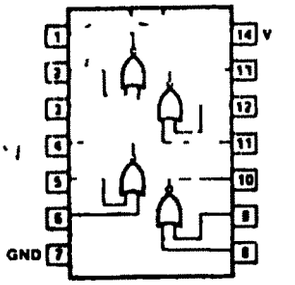
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		8.0		16.9		16		1.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		22		40		36		4.4		V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay	22 15		10 10		2.0 2.0	4.5 5.0	10 10		ns	Figs. 3-1, 3-4	

*DC limits apply over operating temperature range, AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7402
54S/74S02
54LS/74LS02

QUAD 2-INPUT NOR GATE

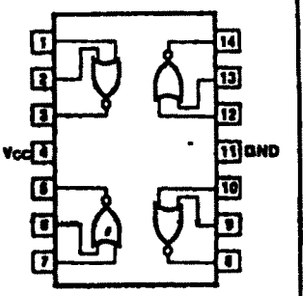
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7402PC, 74LS02PC 74S02PC		9A
Ceramic DIP (D)	A	7402DC, 74LS02DC 74S02DC	5402DM, 54LS02DM 54S02DM	6A
Flatpak (F)	A	74LS02FC, 74S02FC	54LS02FM, 54S02FM	3I
	B	7402FC	5402FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		16		29		3.2	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			27		45		5.4		V_{IN} = Open	
t_{PLH}	Propagation Delay		15	2.0	5.5		10	ns	Figs. 3-1, 3-4	
t_{PHL}			15	2.0	5.5		10			

*DC limits apply over operating temperature range. AC limits apply at T_A = +25°C and V_{CC} = +5.0 V

54/7404
54H/74H04
54S/74S04
54S/74S04A
54LS/74LS04
HEX INVERTER

ORDERING CODE: See Section 9

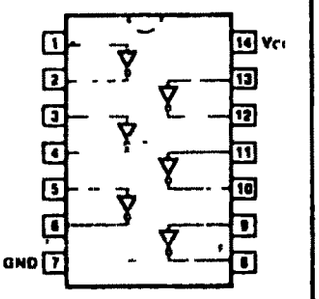
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7404PC, 74H04PC 74S04PC, 74S04APC 74LS04PC		9A
Ceramic DIP (D)	A	7404DC, 74H04DC 74S04DC, 74S04ADC 74LS04DC	5404DM, 54H04DM 54S04DM, 54S04ADM 54LS04DM	6A
Flatpak (F)	A	74S04FC, 74H04AFC 74LS04FC	54S04FM, 54S04AFM 54LS04FM	3I
	B	7404FC, 74H04FC	5404FM, 54H04FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

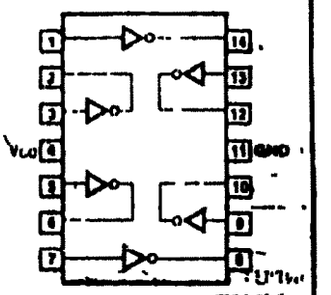
PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAMS

PINOUT A



PINOUT B



DC AND AC CHARACTERISTICS: See Section 3*

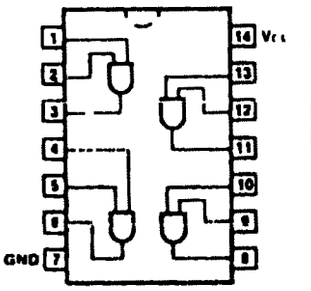
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		12		26		24		2.4	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		33		58		54		6.6		V_{IN} = Open	
t_{PLH}	Propagation Delay		22		10	2.0	4.5		10	ns	Fig. 3-1, 3-4	
t_{PHL}			15		10	2.0	5.0		10			
t_{PLH}	Propagation Delay (54/74S04A only)					1.0	3.5			ns	Fig. 3-1, 3-4	
t_{PHL}						1.0	4.0					

*DC limits apply over operating temperature range. AC limits apply at T_A = +25°C and V_{CC} = +5.0 V

54/7408
54H/74H08
54S/74S08
54LS/74LS08

QUAD 2-INPUT AND GATE

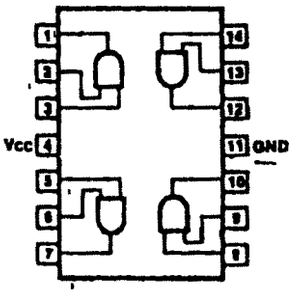
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE Vcc = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE Vcc = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7408PC, 74H08PC 74S08PC, 74LS08PC		9A
Ceramic DIP (D)	A	7408DC, 74H08DC 74S08DC, 74LS08DC	5408DM, 54H08DM 54S08DM, 54LS08DM	6A
Flatpak (F)	A	7408FC, 74S08FC 74LS08FC	5408FM, 54S08FM 54LS08FM	3I
	B	74H08FC	54H08FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. Definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

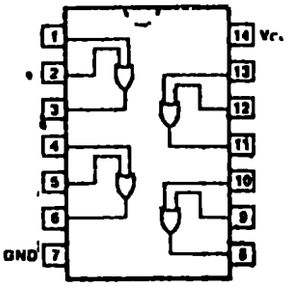
DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		21		40		32		4.8	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}	Current		33		64		57		8.8		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		27		12	2.5	7.0		13	ns	Fig. 3-1, 3-5	
t_{PHL}			19		12	2.5	7.5		11			

*DC limits apply over operating temperature range, AC limits apply at T_A = +25°C and V_{CC} = +5.0 V

54/7432
54S/74S32
54LS/74LS32
QUAD 2-INPUT OR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V +10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7432PC, 74S32PC 74LS32PC		9A
Ceramic DIP (D)	A	7432DC, 74S32DC 74LS32DC	5432DM, 54S32DM 54LS32DM	6A
Flatpak (F)	A	7432FC, 74S32FC 74LS32FC	5432FM, 54S32FM 54LS32FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3 for U.L. definitions

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS	
		Min.	Max	Min	Max	Min	Max			
I_{CCH}	Power Supply Current		22		32		6.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			38		68		9.8		V_{IN} = Gnd	
t_{PLH} t_{PHL}	Propagation Delay		15 22	2.0 2.0	7.0 7.0		15 15	ns	Figs. 3-1, 3-5	

*DC limits apply over operating temperature range. AC limits apply at T_A = +25°C and V_{CC} = +5.0 V

UNIT LOADS (U.L.) Cont'd

To extend the example, this amount of loading can be driven by any one of the hex inverters in the Commercial grade [illegible] outputs have [illegible] abilities greater than 4.0/3.75. In the Military grade, however, the [illegible] has a rated output LOW drive factor of only 2.5 and thus could not be guaranteed to drive 3.75 unit loads [illegible] selected for operation over the Military temperature range.

[illegible] are open collector [illegible] are also capable of supplying leakage current or of establishing a V_{OH} [illegible] supply and thus the abbreviation XC is substituted. It is assumed that [illegible] resistor value that will establish the desired V_{OH} while supplying the [illegible] leakage current of the subject outputs. In the case of wired [illegible] current Family DC characteristics table or on the data sheet.

ABSOLUTE MAXIMUM RATINGS (Beyond which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature [illegible]	-55°C to +125°C
Junction Temperature Under Bias	-55°C to +175°C
[illegible] Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage[2]	
Emitter Inputs	0.5 V to +5.5 V
LS-TTL[3] Diode and pnp [illegible]	0.5 V to +15 V
Input Current[2,4]	-30 mA to +5.0 mA
Voltage Applied to Outputs in [illegible] State	
Open Collector	0.5 V to +7.0 V
Standard TTL, H-TTL, S-TTL, LP-TTL	0.5 V to V_{CC} Value
Standard LS-TTL[5] (with recommended operating V_{CC})	0.5 V to +10 V
3-State LS-TTL (with V_{CC} = 0 V)	0.5 V to +5.5 V
Current Applied to Outputs in LOW State (Max)	twice the rated I_{OL}

RECOMMENDED OPERATING CONDITIONS[1]

	Min	Max
Free Air Ambient Temperature		
Military (XM)	-55°C	+125°C
Commercial (XC)	0°C	+70°C
Supply Voltage		
Military (XM)	+4.5 V	+5.5 V
Commercial (XC)	+4.75 V	+5.25 V

NOTES

1. Unless otherwise restricted or extended by data specifications.
2. Either input voltage limit or input current limit is sufficient to protect inputs.
3. Refer to input breakdown test in 54LS/74LS family DC Characteristics or individual data sheets for emitter type LS-TTL inputs.
4. Except 9316, 74611 [illegible] mA in [illegible] mA. A pin steady state clamp diode currents greater than 2.0 mA in LS-TTL inputs can cause logic malfunctions. See discussion in the text.
5. Except LS00, LS02, LS04, [illegible], LS74, LS86, LS109, LS112, LS113 and LS114 limited to 0.5 V to +V_{CC} Value.

DC CHARACTERISTICS TABLES

Most of the circuits described in this data book were designed within the general framework of one of the distinctive families of TTL circuits i e TTL H-TTL S-TTL LP TTL or LS-TTL Many dc specifications are common to almost all circuits of a particular family, e g V_{IH} V_{IL} V_{OH} V_{CD}, etc and to avoid needless repetition these common parameters do not appear in the individual data sheets On the following pages are tables of dc characteristics containing the parameter limits and conditions common to the various families of TTL circuits These are intended to augment the distinctive parameters such as ac characteristics input loading, fan-out and power supply cur t listed on the individual data sheets In some cases a particular circuit will depart from its family characteristics in one or more parameters and in these cases the limits or conditions shown on the individual data sheets take precedence over the values listed in the family characteristics table

54XX, 74XX, 93XX & 96XX FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage		2 0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0 8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1 5	V	Min	I_{IN} = -12 mA
V_{OH}	Output HIGH Voltage		2 4	3 4		V	Min	I_{OH} = 40 µA Multiplied by Output HIGH U L Shown on Data Sheet
V_{OL}	Output LOW Voltage			0 2	0 4	V	Min	I_{OL} = 1 6 mA Multiplied by Output LOW U L Shown on Data Sheet
I_{IH}	Input HIGH Current	1 0 U L			40	µA	Max	I_{IH} = 40 µA Multiplied by Input HIGH U L Shown on Data Sheet, V_{IN} = 2 4 V
		2 0 U L			80			
		n U L			n(40)			
	Input HIGH Current Breakdown Test All Inputs				1 0	mA	Max	V_{IN} = 5 5 V
I_{IL}	Input LOW Current	1 0 U L			-1 6	mA	Max	I_{IL} 1 6 mA Multiplied by Input LOW U L Shown on Data Sheet, V_{IN} = 0.4 V
		2 0 U L			-3 2			
		n U L			n(-1 6)			
I_{OH}	Output HIGH Current Open-Collector				250	µA	Min	V_{OH} 5 5 V
I_{OZH}	3-State Output OFF Current HIGH				40	µA	Max	V_{OUT} 2 4 V
I_{OZL}	3-State Output OFF Current LOW				-40	µA	Max	V_{OUT} 0 4 V
I_{OS}[6]	Output Short Circuit Current	Gates 54XX	20		-57	mA	Max	V_{OUT} 0 V
		Gates 74XX	-18		-57			
		Buffers 54XX	-20		-70			
		Buffers 74XX	18		-70			
		93XX	20	-	-70			

Notes on following pages

93L FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage		2 0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage	Mil			0 7	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
		Com			0 8			
V_{CD}	Input Clamp Diode Voltage				-1 5	V	Min	I_{IN} = -10 mA
V_{OH}	Output HIGH Voltage		2 4	3 6		V	Min	I_{OH} = -400 µA
V_{OL}	Output LOW Voltage	Mil & Com			0 3	V	Min	I_{OL} = 4 8 mA
		Com			0 4	V	Min	I_{OL} = 8 0 mA
I_{IH}	Input HIGH Current	0 5 U L			20	µA	Max	I_{IH} = 40 µA Multiplied by Input HIGH U L Shown on Data Sheet, V_{IN} = 2 4 V
		1 0 U L			40			
		n U L			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				1 0	mA	Max	V_{IN} = 5.5 V
I_{IL}	Input LOW Current	0 25 U L			-0 4	mA	Max	I_{IL} = -1 6 mA Multiplied by Input LOW U L Shown on Data Sheet, V_{IN} = 0 3 V
		0 5 U L			-0 8			
		n U L			n(-1 6)			
I_{OS}[6]	Output Short Circuit Current		-2 5		-25	mA	Max	V_{OUT} = 0 V

1 Unless otherwise noted conditions and limits apply throughout the temperature range for which the particular device type is rated The ground pin is the reference level for all applied and resultant voltages
2 For definitions of symbols and terminology please see Section 2
3 Unless otherwise stated on individual data sheets
4 Typical characteristics refer to T_A = +25°C and V_{CC} = +5 0 V
5 Min and Max refer to the values listed in the table of recommended operating conditions
6 For testing I_{OS} the use of high speed test apparatus and/or sample and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values Otherwise prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests In any sequence of parameter tests I_{OS} tests should be performed last

AC LOADING AND WAVEFORMS

Figure 3-1 shows the ac test load configuration used for circuits of the 54/74, 54/74H and 54/74S families having totem-pole outputs The diodes and resistor are not used for testing circuits of the 54/74LS, 9XXX, 93XX, 93H, 93S 93L 96XX or 96LS families *Figure 3-2* shows the test load configuration for open-collector outputs For SSI gates, R_L and C_L values are listed in the table below For flip-flops and MSI, R_L and C_L values are listed in the column headings of the ac tables on the data sheets *Figure 3-3* shows the test circuit for measuring Enable and Disable times of 3-state outputs R_L and C_L values are given in the column headings of the ac table in the data sheet except in certain tests they are superceded by R_L or C_L values listed in the Test Conditions column of the same table

A pulse generator signal swing of 0 V to +3 0 V, terminated at the test socket, is recommended for ac testing A 1 0 MHz square wave is recommended for most propagation delay tests, with rise and fall times of 2 5 ns for S-TTL 10 ns for LP-TTL and 6 0 ns for circuits of other families The generator PRR must necessarily be increased for testing f_{max} and decreased for testing one-shot pulse widths Two pulse generators are usually required for testing such parameters as set-up time hold time, recovery time etc.

AC LOADS FOR SSI GATES

SSI DEVICES	AC TEST	54/74		54H/74H		54S/74S		54LS/74LS	
		C_L	R_L	C_L	R_L	C_L	R_L	C_L	R_L
'01, '03, '05 '12, '22	t_{PLH} t_{PHL}	15 pF 15 pF	4 kΩ 400 Ω	25 pF 25 pF	280 Ω 280 Ω	15 pF 15 pF	280 Ω 280 Ω	15 pF 15 pF	2 kΩ 2 kΩ
'09, '15, '55	t_{PLH}/t_{PHL}	15 pF	400 Ω			15 pF	280 Ω	15 pF	2 kΩ
'06, '07, '16, '17	t_{PLH}/t_{PHL}	15 pF	110 Ω						
'26	t_{PLH}/t_{PHL}	15 pF	1 kΩ					15 pF	2 kΩ
'28, '33, '37, '38	t_{PLH}/t_{PHL}	45 pF	133 Ω					50 pF	667 Ω
'40, '140	t_{PLH}/t_{PHL}	15 pF	133 Ω	25 pF	93 Ω	50 pF	93Ω	50 pF	667 Ω
'125, '126, '365 '366, '367, '368	t_{PLH} HL, ZL, ZH t_{PHZ} LZ	50 pF 5 pF	400 Ω 400 Ω					50 pF 5 pF	667 Ω 667 Ω
'134	t_{PLH}/t_{PHL} t_{PZH}/t_{PZL} t_{PHZ}/t_{PLZ}					15 pF 50 pF 50 pF	280 Ω 280 Ω 280 Ω		
All Standard Gates with Totem Pole Outputs	t_{PLH}/t_{PHL}	15 pF	400 Ω	25 pF	280 Ω	15 pF	280 Ω	15 pF	—

54/7474
54H/74H74
54S/74S74
54LS/74LS74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '74 devices are dual D-type flip-flops with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

TRUTH TABLE
(Each Half)

INPUT	OUTPUTS	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

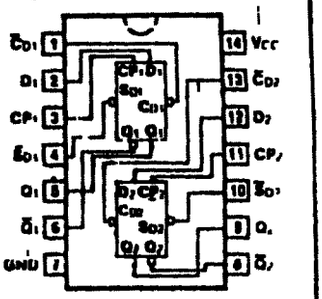
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

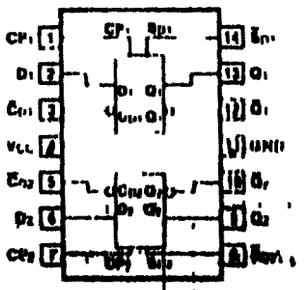
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7474PC, 74H74PC 74S74PC, 74LS74PC		9A
Ceramic DIP (D)	A	7474DC, 74H74DC 74S74DC, 74LS74DC	5474DM, 54H74DM 54S74DM, 54LS74DM	6A
Flatpak (F)	A	74LS74FC, 74LS74FC	54S74FM, 54LS74FM	3I
	B	7474FC, 74H74FC	5474FM, 54H74FM	

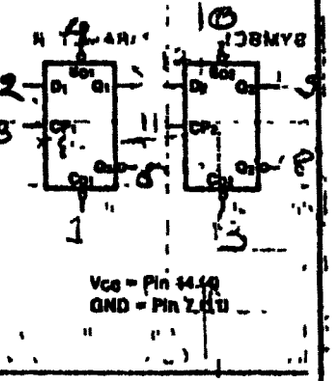
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



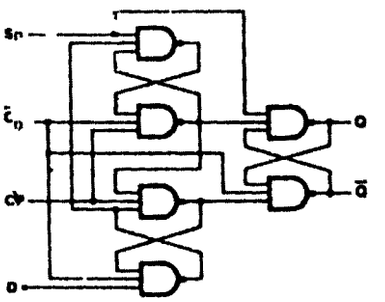
LOGIC SYMBOL



INPUT LOADING/FAN-OUT See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D_1, D_2	Data Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	2.0/2.0	2.5/2.5	2.5/2.5	1.0/0.5
$\bar{C}_{D1}$, $\bar{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/1.0	3.75/2.5	3.75/3.75	1.5/0.75
$\bar{S}_{D1}$, $\bar{S}_{D2}$	Direct Set Inputs (Active LOW)	2.0/1.0	2.5/1.25	2.5/2.5	1.0/0.5
Q_1, $\bar{Q}_1$, Q_2, $\bar{Q}_2$	Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		30		42		50		8.0	mA	V_{CC} = Max., V_{CP} = 0 V
		XC		30		50		50		8.0		

AC CHARACTERISTICS. V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74H C_L = 25 pF, R_L = 280 Ω Min	54/74H Max	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	15		35		75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\bar{Q}_n$	25 40		15 20		9.0 11		25 35		ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q_n or $\bar{Q}_n$	25 40		20 30		8.0 13.5		15 35		ns	$V_{CP} \geq 2.0$ V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q_n or $\bar{Q}_n$	25 40		20 30		6.0 8.0		15 24		ns	$V_{CP} \leq 0.8$ V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max	Min	Max		
t_s (H)	Setup Time HIGH D_n to CP_n	20		10		3.0		10		ns	Fig. 3-6
t_h (H)	Hold Time HIGH D_n to CP_n	5.0		0		0		5.0		ns	
t_s (L)	Setup Time LOW D_n to CP_n	20		15		3.0		20		ns	Fig. 3-6
t_h (L)	Hold Time LOW D_n to CP_n	5.0		0		0		5.0		ns	
t_w (H) t_w (L)	CP_n Pulse Width	30 37		15 13.5		6.0 7.3		18 15.5		ns	Fig. 3-8
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	30		25		7.0		15		ns	Fig. 3-10

54S/74S113
54LS/74LS113

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION The 113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum set-up and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

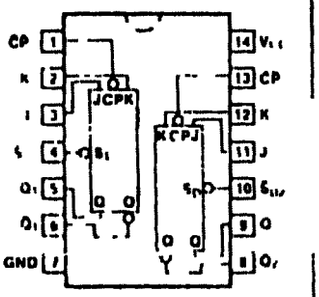
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

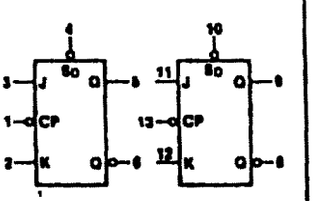
Asynchronous Input
LOW input to $\bar{S}_D$ sets Q to HIGH level
Set is independent of clock

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

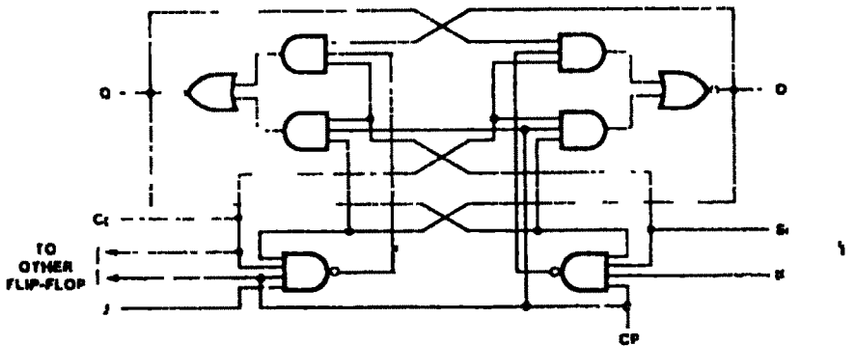
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S113PC, 74LS113PC		9A
Ceramic DIP (D)	A	74S113DC, 74LS113DC	54S113DM, 54LS113DM	6A
Flatpak (F)	A	74S113FC 74LS113FC	54S113FM, 54LS113FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.0	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.5/2.5	2.0/0.5
$\bar{S}_{D1}$, $\bar{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/4.375	1.5/0.5
Q_1, Q_2, $\bar{Q}_1$, $\bar{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		7.0 7.0		16 24	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C_D}$ or $\overline{S_{Dn}}$ to Q or $\overline{Q}$		7.0 7.0		16 24	ns	Figs. 3-1, 3-10

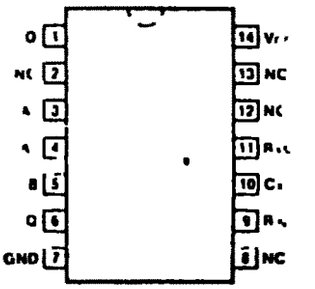
AC OPERATING REQUIREMENTS V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	7.0 7.0		20 15		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0 0		0 0		ns	Fig. 3-7
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	6.0 6.5		20 15		ns	Fig. 3-9
t_w	$\overline{C_D}$ or $\overline{S_{Dn}}$ Pulse Width	8.0		15		ns	Fig. 3-10

54/74121

MONOSTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A



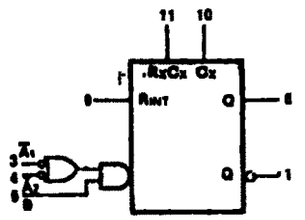
DESCRIPTION — The 121 features positive and negative dc level triggering inputs and complementary outputs Input pin 5 directly activates a Schmitt circuit which provides temperature compensated level detection, increases immunity to positive-going noise and assures jitter-free response to slowly rising triggers

When triggering occurs, internal feedback latches the circuit, prevents re triggering while the output pulse is in progress and increases immunity to negative-going noise Noise immunity is typically 1 2 V at the inputs and 1 5 V on Vcc

Output pulse width stability is primarily a function of the external R_x and C_x chosen for the application A 2 kΩ internal resistor is provided for optional use where output pulse width stability requirements are less stringent Maximum duty cycle capability ranges from 67% with a 2 kΩ resistor to 90% with a 40 kΩ resistor Duty cycles beyond this range tend to reduce the output pulse width Otherwise, output pulse width follows the relationship

$$t_w = 0.69\ R_x C_x$$

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2,8,12,13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5 0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5 0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74121PC		9A
Ceramic DIP (D)	A	74121DC	54121DM	6A
Flatpak (F)	A	74121FC	54121FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{A}_1$, $\overline{A}_2$	Trigger Inputs (Active Falling Edge)	1 0/1.0
B	Schmitt Trigger Input (Active Rising Edge)	2 0/2 0
Q, $\overline{Q}$	Outputs	20/10

TRIGGERING TRUTH TABLE

INPUTS $\bar{A}_1$	INPUTS $\bar{A}_2$	INPUTS B	RESPONSE
H	H	⎍	No Trigger
L	X	⎍	Trigger
X	L	⎍	Trigger
⎺⎺	L	X	No Trigger
L	⎺⎺	L	No Trigger
L	⎺⎺	H	Trigger
L	⎺⎺	X	No Trigger
X	⎺⎺	L	No Trigger
H	⎺⎺	H	Trigger

NOTE

Triggering occurs only when the Q output is HIGH and in timing cycle and one of the above triggering situations is satisfied

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage at $\bar{A}_n$ or B Inputs			2.0	V	V_{CC} = Min
V_{T-}	Negative-going Threshold Voltage at $\bar{A}_n$ or B Inputs		0.8		V	V_{CC} = Min
I_{OS}	Output Short Circuit Current	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-55		
I_{CC}	Power Supply Current	Quiescent State		25	mA	V_{CC} = Max
		Fired State		40		

AC CHARACTERISTICS V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF Min	54/74 C_L = 15 pF Max	UNITS	CONDITIONS	
t_{PLH}	Propagation Delay B to Q	15	55	ns	C_x = 80 pF Fig 3-1, Fig a	
t_{PLH}	Propagation Delay $\bar{A}_n$ to Q	25	70	ns		
t_{PHL}	Propagation Delay B to $\bar{Q}$	20	65	ns		
t_{PHL}	Propagation Delay $\bar{A}_n$ to $\bar{Q}$	30	80	ns		
t_w	Pulse Width Using Internal Timing Resistor	70	150	ns	C_x = 80 pF	R_x = Open Fig 3-1 Fig a Pin 9 = V_{CC}
t_w	Pulse Width with Zero Timing Capacitance	20	50	ns	C_x = 0 pF	
t_w	Pulse Width Using External Timing Resistor	600	800	ns	C_x = 100 pF	R_x = 10 kΩ Pin 9 = Open Fig 3-1, a
		6.0	8.0	ms	C_x = 1.0 μF	
t_{HOLD}	Minimum Duration of Trigger Pulse		50	ns	C_x = 80 pF, R_x = Open Pin 9 = V_{CC}, Fig a	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{r-f}	Input Pulse Rise/Fall Slew Rate	@ A_n		1.0	V/μs	
		@ B		1.0	V/s	
R_x	External Timing Resistor	XC	1.4	40	kΩ	
		XM	1.4	30		
C_x	External Timing Capacitor		0	1000	μF	
t_w	Output Pulse Width			40	sec	Fig. a
	Duty Cycle	XM,XC		67	%	R_x = 2 kΩ
		XM		90		R_x = 30 kΩ
		XC		90		R_x = 40 kΩ

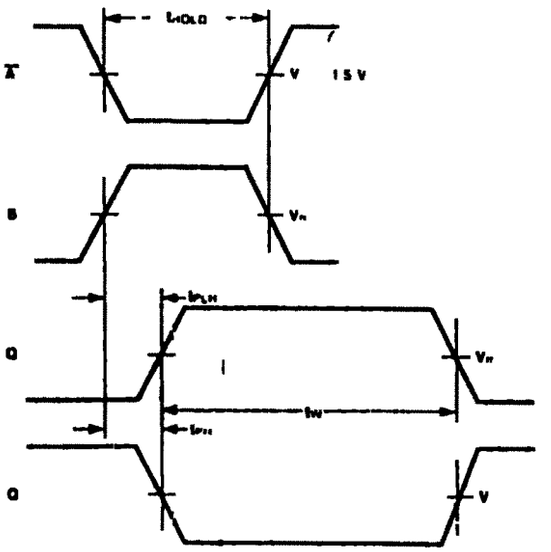


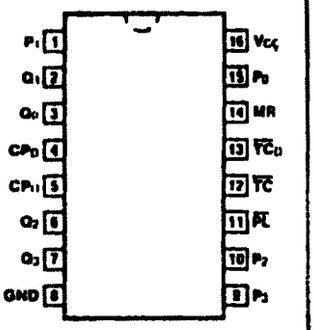
Fig. a

54/74193
54LS/74LS193

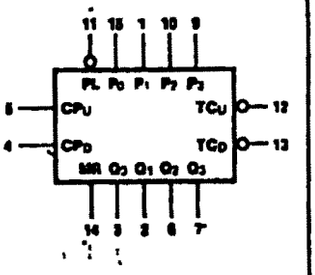
UP/DOWN BINARY COUNTER
(With Separate Up/down Clocks)

DESCRIPTION — The '193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks. For functional description and detail specifications please refer to the '192 data sheet.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74193PC, 74LS193PC		9B
Ceramic DIP (D)	A	74193DC, 74LS193DC	54193DM, 54LS193DM	6B
Flatpak (F)	A	74193FC, 74LS193FC	54193FM, 54LS193FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

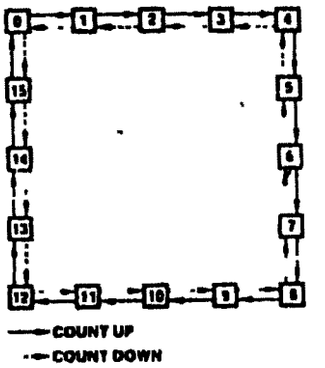
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
CP_D	Count Down Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{TC_D}$	Terminal Count Down (Borrow) Output (Active LOW)	20/10	10/5.0 (2.5)
$\overline{TC_U}$	Terminal Count Up (Carry) Output (Active LOW)	20/10	10/5.0 (2.5)

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn
L	L	X	X	Preset (Asyn
L	H	H	H	No Change
L	H	⌐¬	H	Count Up
L	H	H	⌐¬	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

STATE DIAGRAM

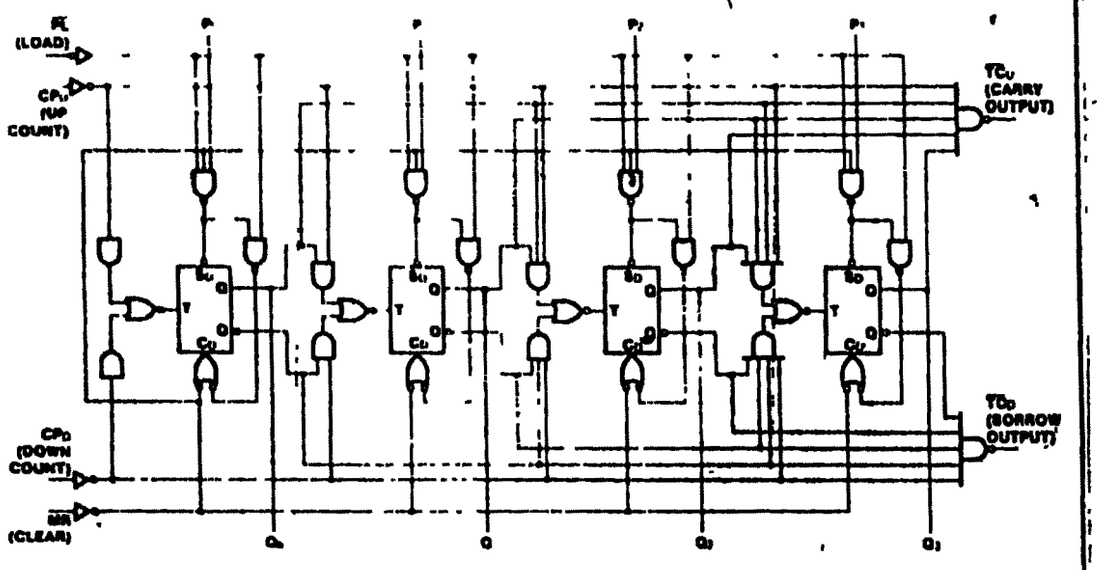


LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \bar{Q}_0 \cdot \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 \cdot \overline{CP}_D$$

LOGIC DIAGRAM



54LS/74LS245

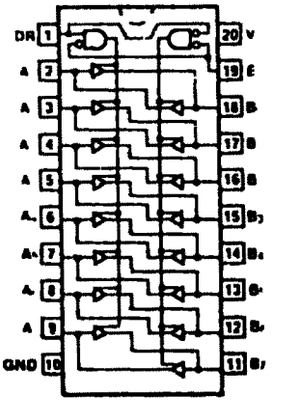
OCTAL BUS TRANSCEIVER

(With 3 State Outputs)

DESCRIPTION [illegible] bus transmitter/receiver designed for [illegible] two way [illegible] between [illegible] data buses. Direction [illegible] transmission of data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input $\overline{E}$ can be used to isolate the busses.

- HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY
- 2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION
- INPUT DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5% T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10% T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS245PC		9Z
Ceramic DIP (D)	A	74LS245DC	54LS245DM	4E
Flatpak (F)	A	74LS245FC	54LS245FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.0		V	I_{OH} = -12 mA	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.0			I_{OH} = -15 mA	
V_{OH}	Output HIGH Voltage		2.4		V	I_{OH} = -3.0 mA, V_{CC} = Min; V_{IN} = V_{IH} or V_{IL} per Truth Table	
$V_{T+} - V_{T-}$	Hysteresis Voltage		0.2		V	V_{CC} = Min	
I_{OS}	Output Short Circuit Current		-40	-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	HIGH		70	mA	V_{CC} = Max	
		LOW		90			
		OFF		95			

AC CHARACTERISTICS V_{CC} = 5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

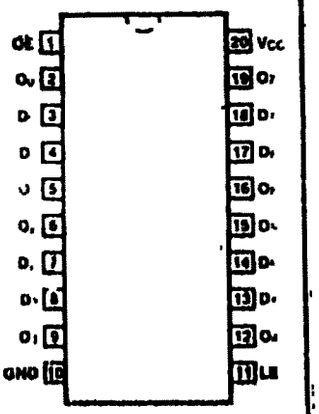
SYMBOL	PARAMETER	54/74LS C_L = 45 pF Min	54/74LS C_L = 45 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Data to Output		18 18	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time		25 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω
t_{PLZ} t_{PHZ}	Output Disable Time		25 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

54LS/74LS373

OCTAL TRANSPARENT LATCH

(With 3-State Outputs)

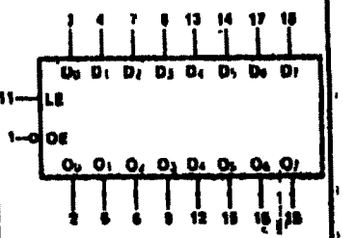
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The 373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5% TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10% TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS373PC		9Z
Ceramic DIP (D)	A	74LS373DC	54LS373DM	4E
Flatpak (F)	A	74LS373FC	54LS373FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_7$	3-State Latch Outputs	65/15 (25)/17.5)

FUNCTIONAL DESCRIPTION — The '373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM