CHAPTER - II

CHAPTER - 2

BACKGROUND DISCUSSION

2.1. DIGITAL STORAGE OSCILLOSCOPE :

Fig. 2.11 and 2.12 are the block diagramatic sketches of a analog and a digital storage oscilloscopes. Various features which are not really transparent through the block diagram comparison are illucidated below.

The storage scopes are always switchable from analog to digital mode. The signal attenuator and pre-amplifiers are common and the analog band-width of the scope is limited by the pre/intermediate amplifiers and the type of CRT used with the scope. As a basic principal in the storage mode the analog signals are sampled with the clock rate proportional to the time base mode selected. The sampled data is A/D converted and store in to the memory of the scope. As large as 1024/2048 samples are acquised per scan [i.e. full horizontal screen width] (4, 18). The triggers are managed at a specified point in the acquised data. The sampled data could be simultaneously or after storage displayed in the selected mode of display. Cursors could be moved on the waveforms to determine and simultaneously display the ΔV, ΔT, values between the cursor locations [Fig.2.13].

Despite of these there are various features which differentiate the analog scope from a digital storage scope. This occurrs because of the additional capabilities of signal

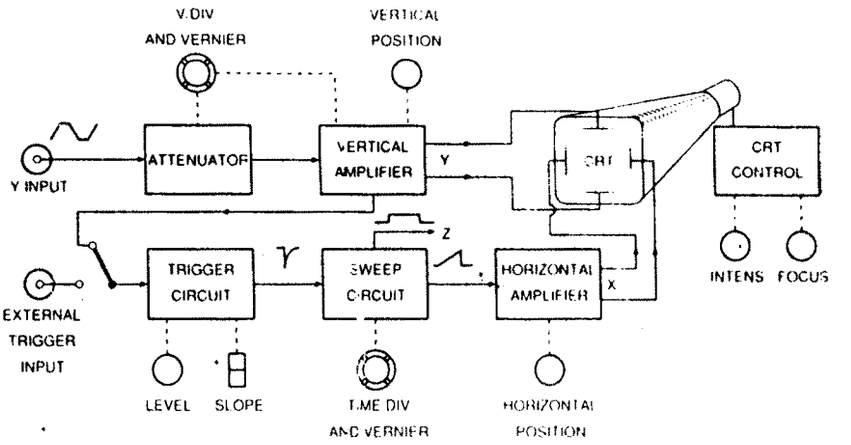


Fig-2-11. BLOCK DIAGRAM OF ANALOG SCOPE.

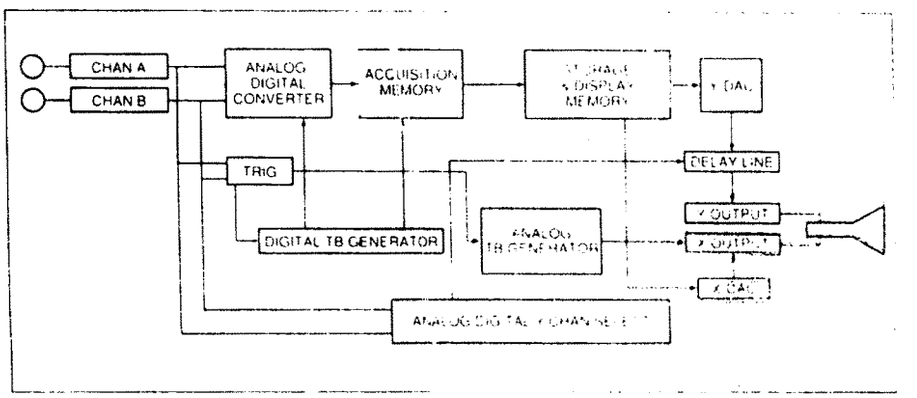


Fig. 2-12 BLOCK DIAGRAM OF DSO.

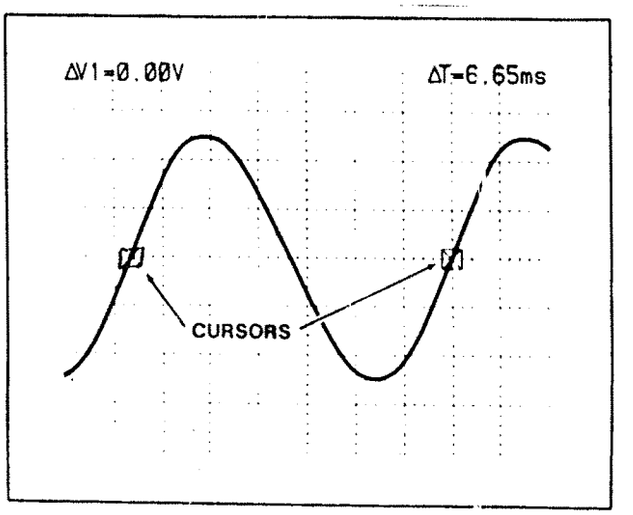


Fig. 2-13 CURSORS DISPLAY

processing and storage through the DSO and its microcomputer support. 1) The DSO allows trigger settings anywhere on the horizontal width of the captured signal and offers pre-trigger and post-trigger views of the waveforms. 2) At each time instance with respective trigger a sampled data pair could be dynamically processed to store corresponding maximum and minimum values of the signal captured, allowing observations of undistorted envelops of amplitude modulated signals. The carrier frequencies could be very nearly equal to 2/sampling rate (19). 3) This mode also adds to the glitch catching capability of the scope, if the maximas and minimas over number of sweeps could be captured and displayed (20). 4) Averaging mode of DSO uses a normalised algorithm to determine and store average values of sampled data corresponding to each memory locations over multiple acquisition cycle and thus could be used to improve amplitude resolutions of a noisy input.

Not only at the level of acquisition but also at the level of displaying the signal various dynamic processing routines could be employed, these are used to smoothen the waveforms displayed. Various interpolation schemes are menu or switch selectable. These include zero-order, first-order, sine, pulse interpolation techniques etc.[Fig.2.14].

As pointed out earlier the sampling clock is proportional to the time-base mode selected. Therefore the device operation characteristically differs in various groups of time-base settings. In the slow mode of time-base the acquisition and display of the signal is effectively simultaneous. In this mode

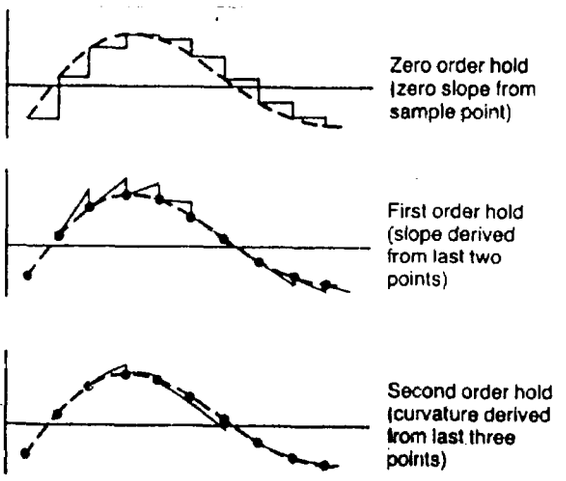
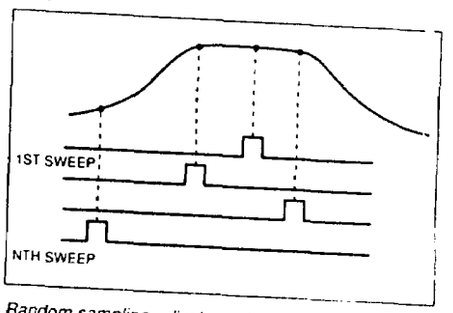
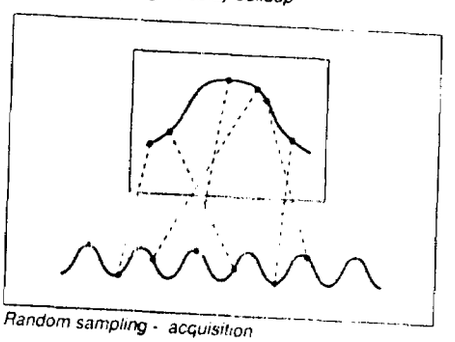


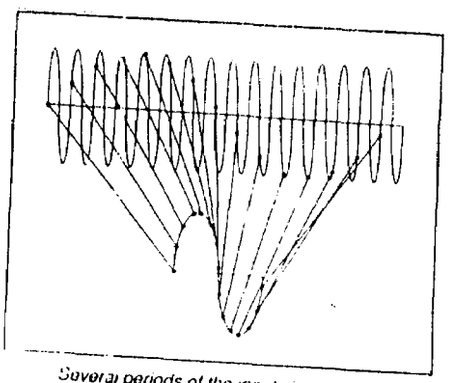
Fig-2.14 INTERPOLUTION TECHNIQS.



Random sampling - display buildup



Random sampling - acquisition



Several periods of the input signal are sampled for reconstruction of the waveform.

Fig-2.15 RANDOM SAMPLING.

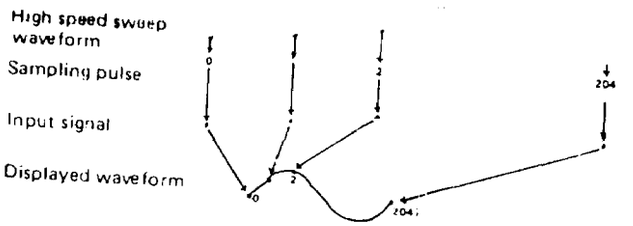


Fig. 2.16 - EQUIVALANT SAMPLING.

the auto-mode selection is meaningless to display the line in absence of the input because of the constraints of persistance of vision and the phosphorous decay of CRT tube and therefore system works effectively in the normal mode.

Stiking to the facilities offered by Tek-2230, the DSO actions within this mode are as below (21). In scan mode with a system operating in a normal trigger mode, the pre-trigger data is updated into the memory and on to the screen upon receipt of trigger the waveform display then scans to the right to offer post trigger event display. If auto-trigger is selected within the scan mode then the scan appears, independent of trigger, continuously. In the roll-mode the latest acquisition appears on the right edge of CRT, the display is updated after each acquisiton. These two modes could also be combined together.

At the faster time-base rates the scope acquises and then displays a full screen information, referred as record mode (18). Dynamic signal processing plays an important role in this mode of time-base. Added to these are the delayed time-base facilities which are effective in both analog and digital storage mode.

The record sample mode could not be expanded for all the s/div settings of the scope. In this range of time-base, the repeatative mode, the philosophy of acquisition and display is characteristically different and needs involved understanding of the sampling process. A limit occurrs at a time-base selection where the maximum sampling frequency of ADC equal to the rate

demanded by s/div settings [i.e. Number of samples/div / s/div], beyond which the number of samples acquised/div can not keep up with the time-base. This occurs because of the limiting sampling frequency of ADC used. The flash A/D convertors offers maximum sampling frequency over the other A/D convertors. CA 3300 and CA 3308 operate at 15MHz clock and capable of producing 15MS/sec at 6-bit and 8-bit resolutions respectively (Appendix-A). Sampling speed could be further improved by using 2 or more ADCs in parallel in the different phases of clock. Similarly the micro-circuit allows increased resolution with the use of multiple chips in parallel.

Recently Philips Inc. (22) has announced a technique of A/D conversion, the folding and interpolution technique, as an alternative to the flash conversion for better performance. The performance is improved by reducing the 2^n comparators to $2^n/4$ and compensating the absence by a resistance ladder, e.g. for a system with 8-bit resolution, the device uses 64 comparators, instead of 256, and a resistance ladder of 256 resistors in output of these comparators. The system is effectively a combination of flash and successive approximation techniques [IC TDA 8703].

Another way out of the situation is also implemented by Philips. They use P^2CCD technology (23) for the purpose and storage bandwidths of as high as 250 MHz is offered. The analog signal is stored on Profiled Peristaltic Charge Coupled Device [P^2CCD] using a clock with too high a speed. Triggers are used to stop the acquisition and then the stored analog signal could be

converted at a slower clock rate of the ADC for storage and displayed. Amongst the other techniques of acquisition for time-base rates beyond sampling rate, two different techniques viz. random and parallel sampling techniques are used for slow and fast repeatation rate samples respectively. In random sampling technique a fast counter is used to measure the time interval between the trigger and the sampling event. This time interval provides a slot for acquisition of samples. Multiple samples are acquised in this slot till the end of the time-base width selected. The process of acquisition is repeated for a statistically estimated number where because of the random occurrence of trigger and sampling clock, all the available slots will filled. The default mode of operation is average in this case. The technique is figurised in Fig.2.15.

In parallel or equivalent sampling technique the triggers are used to run the time base. Simultaneously a stare-case signal is also generated. Amplitude max. of the stare-case and the time-base signal are equal and on cross-point of time-base and stair case, the samples are acquised. After all the steps of stair are used to sample the signal, the acquisition is complete. [Fig.2.16.]

Both these techniques demand the input signal to be repeatative. Owing to these fact the hold time in the DSO is sufficiently large and the signal and information displays are executed within the hold-time (24). The acquisiton and display is treated as a two separate action events.

2.2. DESIGN AND TIMING OF HARDWARE LOGIC SYSTEM :

Present attempt is towards elaborating various intricacies of loading and timing constraints encountered while interfacing multiple digital logic components (IC's) together to form a functional unit.

Within the development stages of microsystem [μs] design, the overall hardware requirement becomes transparent after sagrigation of the task at software [SW] and hardware [HW] levels. Selection of microprocessor [μp] to execute the task plays a crucial role at the stage of task sub-division. The process is interactive and successive steps of HW and the SW design itteratively refine the problem defination to realise a system with optimum performance.

A generalised comparison of all logic families available commercially has been given (25, 26). To illucidate upon various parameters oat to be considered while designing a HW logic unit we would make use of SN74 series, TTL products, as an exemplary logic family. Further the discussion emphasises a few salient features which do not usually form part of any standard text or design data book.

1) Design with TTL Product :

While devicing a real time operating digital system, delays encountered in each sub-logic unit and the loading factors are to reconcile with the descret nature of the analog signal to be

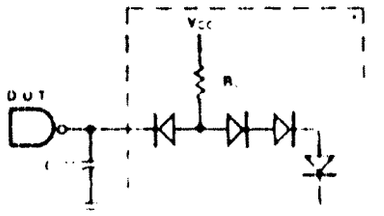
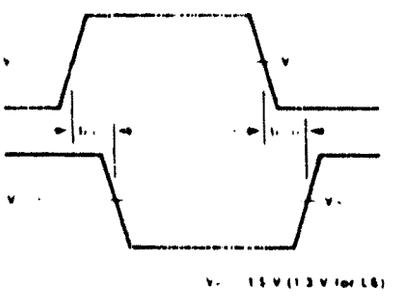
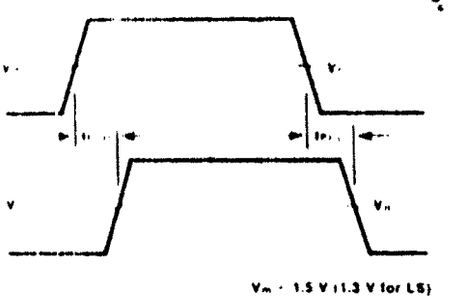


Fig. 3-21 Test Load for Totem Pole (Tri-State) Tri-State Mode



V_m = 1.5 V (1.3 V for LS)

Fig. 3-22a Waveform for Inverting Functions



V_m = 1.5 V (1.3 V for LS)

Fig. 3-22b Waveform for Non-Inverting Functions

LOADING, SPECIFICATIONS AND WAVEFORMS

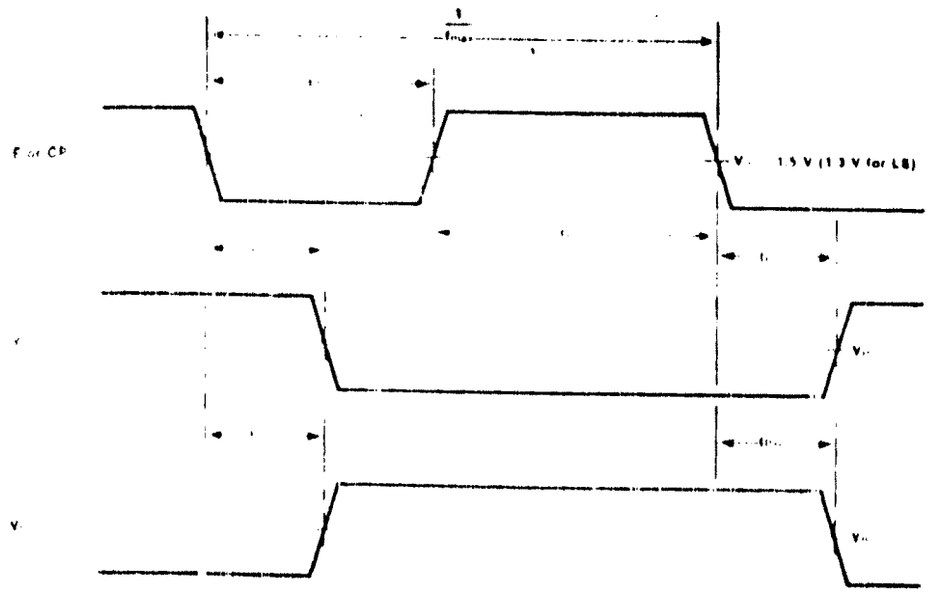


Fig. 3-23 Propagation Delays from Falling-Edge Clock or Enable

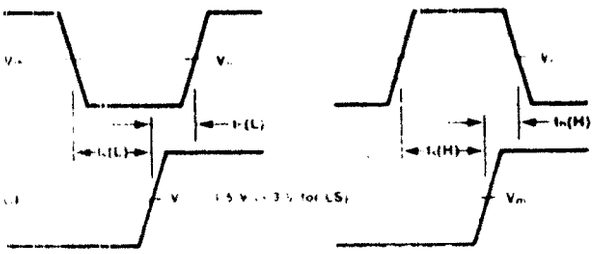


Fig. 3-21a Set-up and Hold Times, Rising-Edge Clock

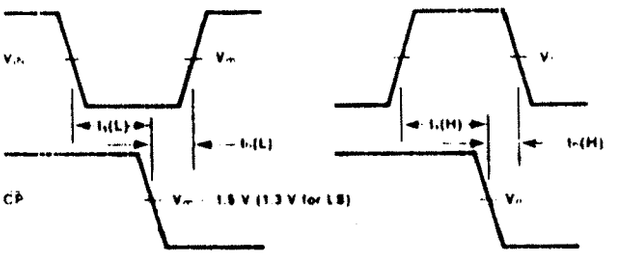


Fig. 3-21b Set-up and Hold Times, Falling-Edge Clock

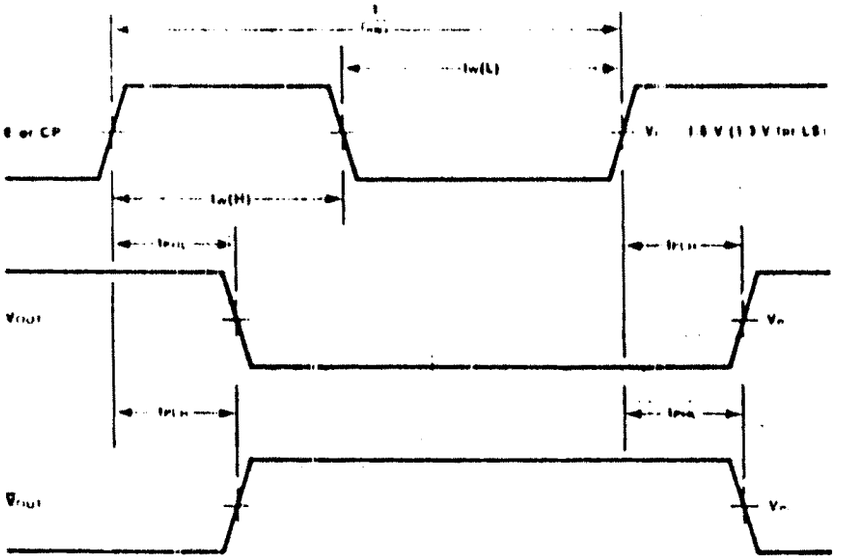


Fig. 3-22 Propagation Delays from Rising-Edge Clock or Enable

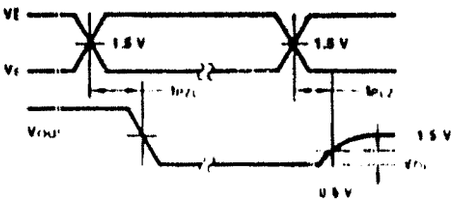


Fig. 3-21 3-State Output LOW Enable and Disable Times

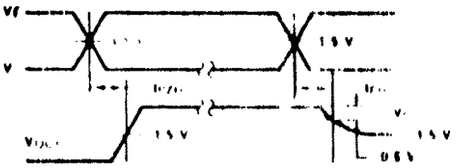


Fig. 3-22 3-State Output HIGH Enable and Disable Times

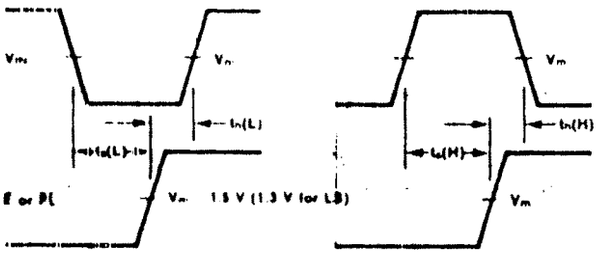


Fig. 3-23 Setup and Hold Times to Active LOW Enable or Parallel Load

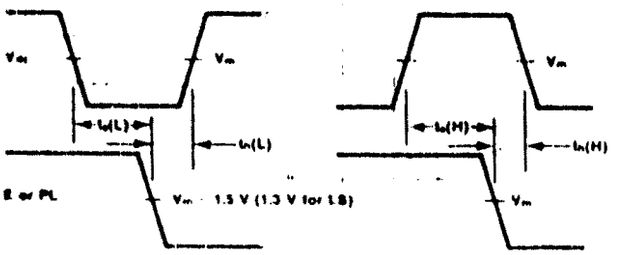


Fig. 3-24 Setup and Hold Times to Active HIGH Enable or Parallel Load

processed and/or timing [margin] requirements of occurrance of events, etc. A clock signal is used, to provide basic timing for various real time logic operations.

To develope greater insight in to the delays and timing of logic operations performed by standard TTL logic ICs, timing diagrams have been given and corresponding data of logic family component is also shown with Fig.2.22a to 2.22j.

All the diagrams are with respective standard test load of 10 gates, Temp 25^{o}C and, Vcc +5 volts. (Fig. 2.21).

The rise and fall times, propogation delay and other timings are dependent on the ambient temp. and with effective loading capatitance (27). The typical average propogation delay time with respect to the temp. and the capacitive loading is as shown in Fig. 2.23, 2.24 respectively.

Texas Instruments Incorporation, the originator of the TTL logic family, has published a design guide book. Here a chapter is devoted for noise consideration (28). Right from the grounding and decoupling effects, effects of power supply bypass capacitance, stray capacitance of the PCB and loading capacitance on the Vo, Vcc and Ic are discussed in details. Further the transmission line interconnection and clock cross-talk are also important to be given consideration to. Various circuits have been designed to reduce the cross-talk. Being too standard a design guide line these effects are not elaborated in the dissertation.

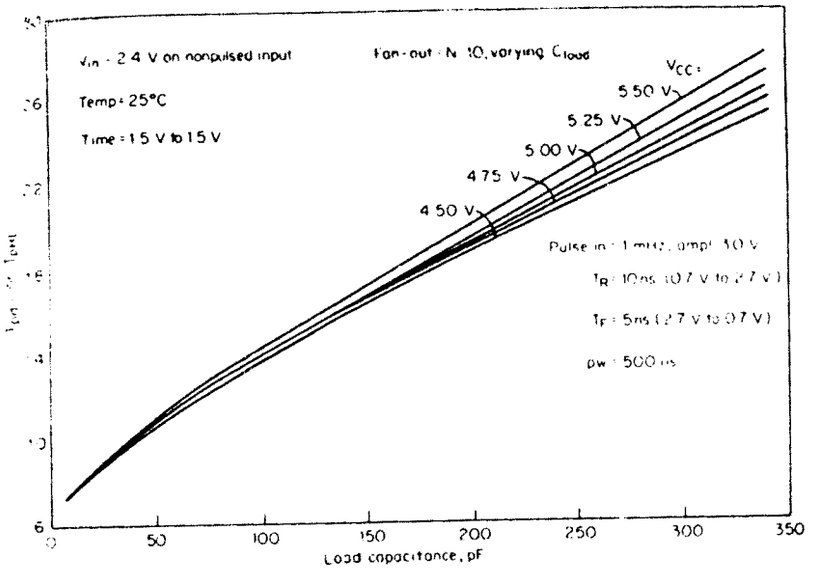


Fig-2.23. TYPICAL PROPAGATION DELAY TIME, FOR SN7400

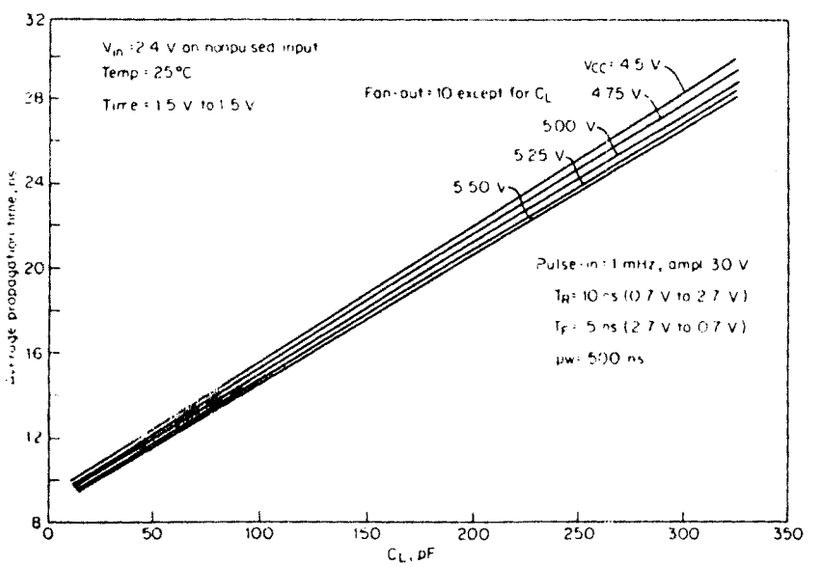


Fig-2.23' TYPICAL PROPAGATION DELAY,

AVERAGE OF t_{pLH} & t_{pHL} FOR SN7400.

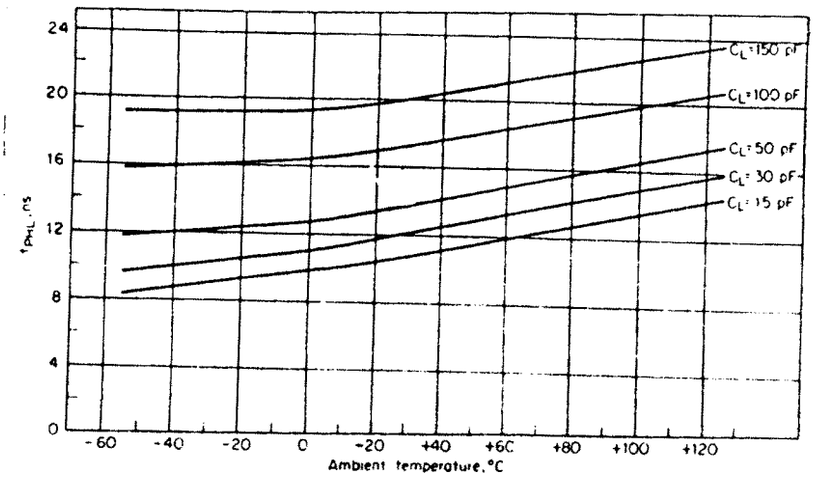


Fig. 2.24 - Typical propagation delay time to logical 1, for SN5400.

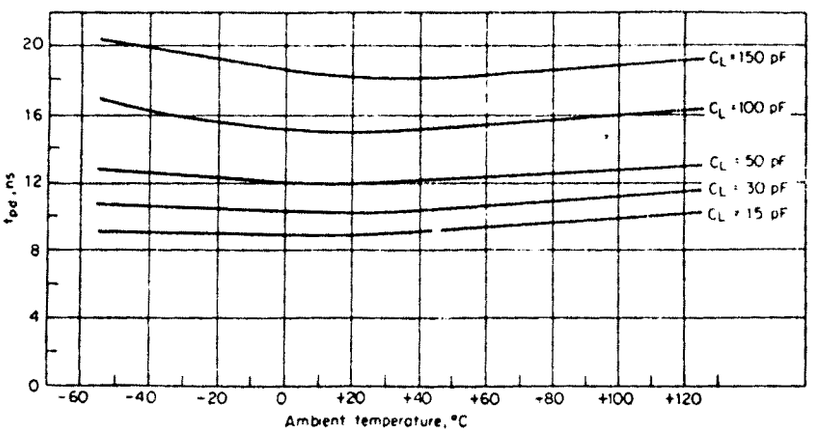


Fig. 2.24' Typical propagation delay, average of t_{PLH} and t_{PHL}, for SN5400.

Unless having thorough understanding of these parameters, the digital system design would be impractical. In various combinational and sequential logic blocks, the timing requirement may become crucial at too high a speed of operation. Further the variation, within limits, of various delay parameters may pose a creatical problem. In these situations additional capacitive loads could be judiciarialy introduced in the logic outputs, such that the delay requirements of the functional logic are satisfied.

Another aspect of the timing is the maximum toggle frequency [fmax] which is applicable only for the device with storage elements [i.e. flip-flops, registers, counters, and latches], as these require a positive feedback. As a consequence of this feedback the clock input of storage device can not receive the clock pulses with spacing closer than the time required for the entire feedback loop to be transversed. Maximum clock frequency is given by fmax = 1/2tpd Hz [where tpd is average propogation time].

Requirement of set up [ts], recovery [tr] and hold [th] times, (Fig. 2.2b, 2.2c), could be used to calculate maximum operating frequency = 1/ts + th, [tr is usually zero]. No doubt along with maximum frequency of operation ts and th is also to be given a consideration to.

The SN74 series, products are available as 74H, 74S, 74LS - etc. (29) where the timing and load consideration for each subsystem are different. Utility of these subsystems is discussed

in the design data book. To satisfy the timing requirements, designers may need to intercombine these subsystem componants together. For the sake of reference loading parameters of these systems are tabulated. (Table 2.21).

Table 2.21

Input Loading/Fanout in terms of Unit Loads.

Pins	74 (U.L.)		74H (U.L.)		74S (U.L.)		74LS (U.L.)	
	High	Low	High	Low	High	Low	High	Low
Input	1.0	1.0	1.25	1.25	1.25	1.25	0.5	0.25
Output	20	10	12.5	12.5	25	12.5	10	5.0

Any form of design is a creative pursuit, and only after defining and analysing the requirements one can involve in the designing process. Real test of the circuit would be, how the circuit performances with time. For this purpose the most convenient method of displaying the changing dynamic situation is to draw the timing diagrams of operations. While drawing the timing diagram one uses the delay times specified by the manufacture. Both the maximum and minimum delay times are required to be treated, as per the need of the circuit. Reconciliation with maximum and minimum time delays in turn define the time margin. [Here the timing performance is assumed estimated on the basis of a event clock as time reference.] In any situation, provision of sufficient margin avoid any kind of race situation and the hazards their concerned. For example, reference is made to the timing diagrams of Fig. 3.32b. 2) ECL Products and ECL to TTL Interface :

Usually for the clock frequencies above - 30 MHz the 74LS series products will be of no utility. Use of 74S series components can not extend these frequencies beyond - 60MHz. Further the available range of products in the 74S series is meagre as compaired to the 74 or 74LS series. Therefore it is imperative to think of faster logic families like ECL. Motorola Semiconductor Corporation has launched two ECL series viz. 1K and 10K. With ECL logic family 1K, frequency of operation could be extended to - 160MHz or more, while 10K series products accomodate clocks up to 1-2GHz. Neverthless, operations at too high a frequency poses a critical requirement of lay-outing the circuit on PCB, transmission line and noise effects their concerned.

The ECL, being a non-saturated logic, offers the propogation delay as low as one or fraction of a nsec. Further the power supply requirement of these components is - 5.2volts. The system uses the positive logic and Fig. 2.25 shows the characteristics of the 1K series product.

Within the functional logic unit all the tasks may not operate at frequencies above 30MHz [limit for 74LS series products]. Additionally a variety of microprocessor is available where the signals are TTL compatable. The designer is delighted because of availability of TTL to ECL and ECL to TTL interface products available commercially e.g. 10124, 10125 (Appendix). Therefore within the task sub-division, the high frequency [>30 MHz] tasks could be delegated to the ECL logic systems and then the slow and fast logic subsystem could be interfaced.

2.3. SELECTION OF THE PROCESSING UNIT :

To provide overview of the available microprocessors and their utilities a few systems and their salient features have been tabulated (Table 2.31). The classification is on the basis of word length. The tabulation instead being exhaustive is examplary.

Table 2.31

Comparative charts of some microprocessors.

Device	MC2900	MC10800	Am29116	8048	8022	8085	6502	2920	MC68000
Type	Bitslice	Bitslice	Bitslice	uC	uC	Std.	Std.	An.Sig.	Std.
Technology	TTL	ECL	TTL	NMOS	NMOS	HMOS	NMOS	TTL	HMOS
Clock	8MHz	10MHz	10MHz	6MHz	3.6MHz	3MHz	1MHz	10MHz	4MHz
Cycle Time	125ns	100ns	100ns	2.5 us	8.4 us	1.3 us	2.0 us	400ns	400ns
Data Lines	4bit [may be extended]		4bit	8bit	8bit	8bit	8bit	--	16bit
Interrupt	--	4level intr.	--	--	--	4Vector 1NMI	1mask 1NMI	--	7level intr.
Remarks	High Speed appln.	High Speed appln.	Uses bitslice philosophy	Sirgle chip	On chip ADC	Register oriented	Memory oriented	On chip ADC & DAC	--

The bit slice processors usually come-up as multichip configuration and the components are ALU chip, Micro-program sequencer chip, look ahead carry generator etc. The system is intended to kater needs of high speed processing and are available in the TTL or ECL logic forms (MC 2900 series, MC 10800) (30). The average speed of instruction execution lies in the range of few

100 nsec. The slices could be parallely combined to form a processing unit of variable word length. Further a 16-bit slice configuration is also made available from Advanced Micro-Devices (i.e. 29116). The device is utilised in situations where chip count is not a constraint but high execution speeds are required.

Development of software for these devices is rather tedious, oving to its micro-programmability. Despite the widest flexibility offered by micro-instructions and available development aid [MACE 29/800] the software overhead is sufficiently large in these systems.

A subtle point to be noted is that the high speed transfer of DMA type does not really contribute to the requirement of high processing speed. Special purpose DMA circuits (e.g. Am 2964) are made available for this purpose.

The requirement of digital storage scope is mainly of DMA type and therefore we did not opt for the bit slice processors to form a control unit. Neverthless, if real-time data processing is to be additionally included in the DSO, to form a dynamic signal analyser, bit slice device could only be the choice.

The single chip microcomputer configurations are of extremely low chip count. Despite of the reduced chip count, the microcomputers like Intel 8022, 2920, provide on chip ADC and/or DAC facility additionally, to process analog signals directly. The A/D conversion is achieved using successive approximation method, which is inherently slow as compared to the flash conversion.

Therefore for the sampling requirements of 10MS/sec or high these did not form the choice.

As pointed out in Chp. 1 and Sec.2.1, requirement of processing unit for the DSO interface is the elegant interrupt handling facility and not the processing speed. Further, as no dynamic data processing is involved and sufficient hold-off time is acceptable, we have opted for Intel 8085 to form the processing unit. No doubt, the selection is temporarily valid and in the further stages of development of the system, as pointed out earlier we may adopt 2900 or 10800 system.

The Intel 8085 is product of HMOS technology and supports four vectored and a non-vectored interrupt request. Therefore no additional interrupt controller overhead is necessary as far as present interface is concerned. Being a registor oriented processor, temperary operands could be hold in the processor itself and saves the data transfer time. Support for algebric operations is also remarkable and has been found sufficient to kater the requirements of mode selection and operation controls. This would be evident in the forth coming discussion [Ch. 3, 4].

As an additional advantage the processor being a industry standared, micro-system development boards and cross-assemblers are readily available in the market.

The system used by us to test and develop software support of the system is ILCV-2 development board from `Dynalog Micro Systems', Bombay. It supports a serial monitor; further

serial communication software `Tango' is also available (31). The Tango is a menu driven software utility, supporting up/down loading of the software [Hex code] files. Additionally it does support various debugging controls like single instruction cycle execution, insertion of break points, block transfer etc. A 8085 cross-assembler operating on IBM compatible machines, is also provided with the `Tango' [XASM85.COM] (32). The XASM85 is equipped with the standard assembler directives of memory pre-assignments, reservation of storage locations, creating a program to be loaded from a specific origin etc. It does not support MACRO Assembly facility, but program counter relative jumps, anywhere in the 64K range are possible [e.g. JMP $-5, where $ refers to the contents of PC]. Therefore using a standard word processor the program blocks could be repeated in the text. Effectively this may compensate for the unavailable macro declarations. Further it does support a LOC and ENLOC facility to assemble a code which is ment to be executed after it is moved from load adress to some other execution adress. Load adress for the statements in LOC, ENLOC bracket are continuous with the previous program but the labels and jumps are referred to the address provided with LOC <expression> statement.

The `Tango', XASM85 and ILCV-2 have been fully exploited to develope and test the software.