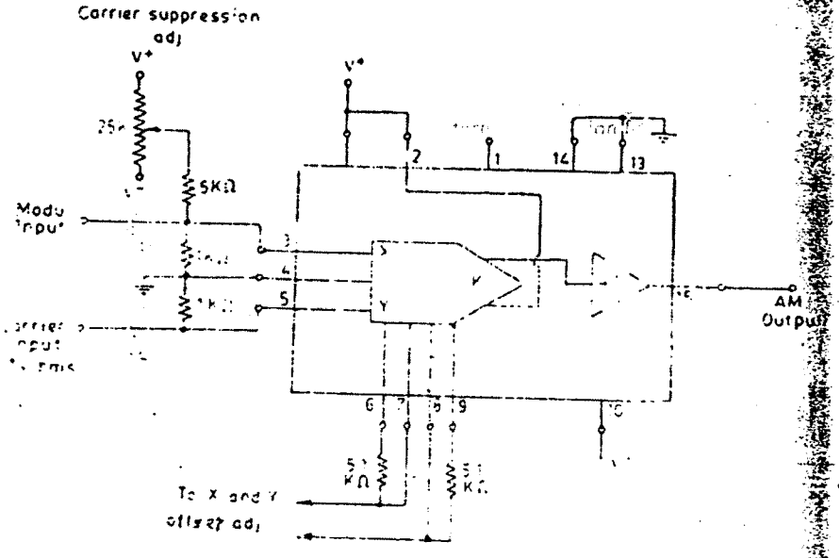
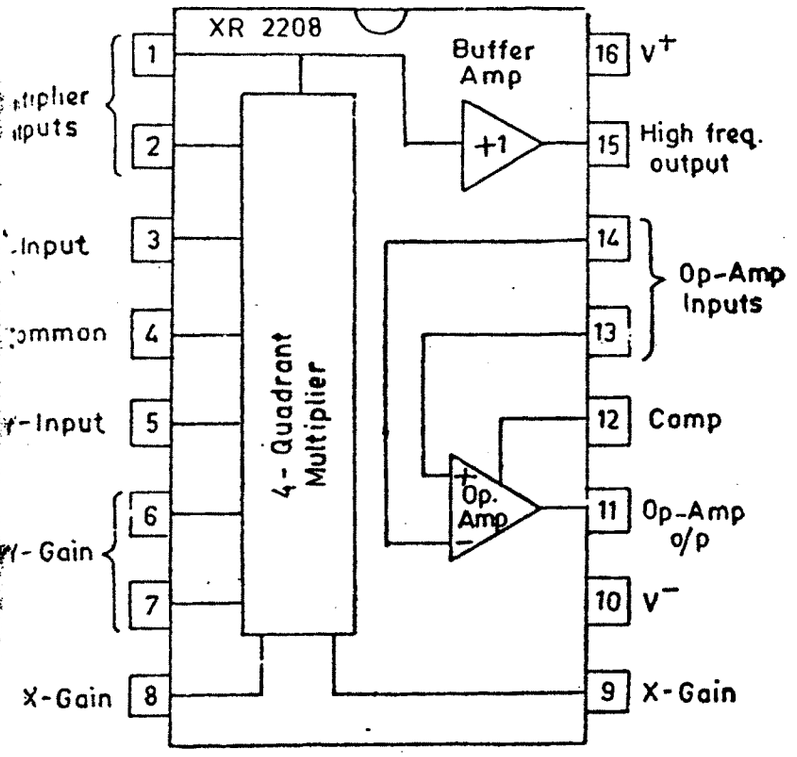
APPENDIX – E

AM Generation and Detection Using Device XR-2208. Fig. 14·57 (*a*) shows a circuit suitable for AM generation, for either suppressed carrier or conventional AM generation. Fig. 14·57 (*b*) shows the pin configuration alongwith internal blocks of the device XR-2208. We should note the primary difference between the two modes of operation. For suppressed carrier AM



(*a*)



(*b*)

Fig. 14·57. Device XR-2208 (*a*) external connection for AM generator (*b*) pin configuration.

generation, the output is at a minimum when the modulation is at a minimum when the modulation is at its zero crossing points and 180° phase reversal occurs in the output when the modulation input goes below this zero crossing point. For conventional AM generation, the output phase does not reverse and the output signal occurs when the modulation input is at its minimum.

Fig. 14·58 (*a*) shows a block diagram scheme for synchronous AM detection and Fig. 14·58 (*b*) shows typical external connections to type XR-2208 which is used as an AM detector.

We have already discussed the block diagram scheme for AM detection as referred to Fig. 14·4 (*e*). In Fig. 14·58 (*a*), however, we have shown two additional blocks which enable to obtain constant amplitude carrier signal from the AM input signal. In this block diagram, before the signal is applied to the *Y* input, it is amplified and limited to convert it to a constant amplitude carrier signal. This carrier signal, as usual, is then multiplied or

mixed with the input signal to produce an output signal that is comprised of the demodulated AM signal alongwith a two-times frequency component (*i.e.*, cos 2 $\omega_c t$ term) as described by Eq. (14·87). The two-time carrier component (cos 2 $\omega_c t$ term) is then filtered out *via* the low-pass filter (LPF), yielding the demodulated output signal.

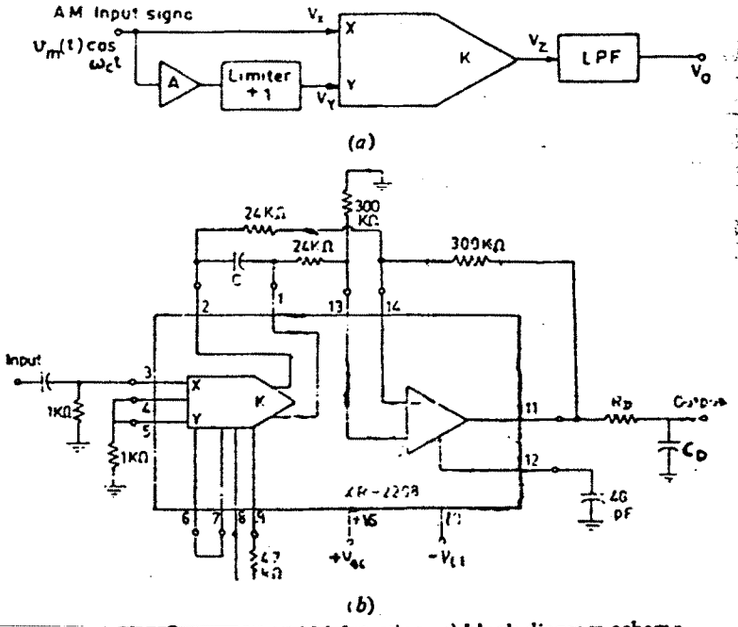


Fig 14·58. Synchronous AM detection *a*) block diagram scheme (*b*) using device XR-2208.

We should note that AM input signal in Fig. 14·58 (*a*) when amplified and limited, a constant amplitude carrier signal is generated of the form

$$V_Y = A_1 \cos \omega_c t + A_2 \cos 3\ \omega_c t + A_3 \cos 5\ \omega_c t + \ldots$$

Since the output will be low-pass filtered, all higher order of this term will be eliminated at this time to yield an input signal.

$$V_Y = A_1 \cos \omega_c t.$$

The synchronous AM detector using XR-2208, as shown in Fig. 14·58 (*b*), is designed for 500 kHz AM detection and modulation signal bandwidth of 20 Hz to 2[illegible] kHz. The output impedance of the multiplier is 10 kΩ between pin 1 and 2.

In Fig. 14·58 (*b*), the *Y* input gain terminals have been shorted to supply maximum gain. This will accomplish both the amplification and limiting to the *Y* input signal. The output filtering is accomplished by connecting a capacitor between the multiplier output terminals.

The cut-off frequency is determined by

$$f_c = \frac{1}{2\pi R_o C}$$

where R_o is the output resistance of the multiplier and C is the filter capacitor value. Since $R_o = 10$ kΩ, then

$$C = \frac{1}{6{\cdot}28 \times 10^4 f_c}$$

Let us choose $f_c = 25$ kHz, so that the two times carrier component (cos 2 $\omega_c t$) will be attenuated by approximately 32 dB. The capacitor value is then given as

$$C = \frac{1}{6{\cdot}28 \times 10^4 \times 25 \times 10^3} = 620 \text{ pF}.$$

The Op-Amp of the device XR-2208 is used to buffer the output signal and to perform the differential-to-single-ended conversion of the multiplier output. R_D and C_D form a post detection filter, which further reduces the two-times frequency component present in the ouput. The cut-off frequency for this filter is also chosen to be approximately 25 kHz. Assuming that the output resistance of the Op-Amp is low, the 3-dB cut-off frequency is determined by

$$f_c = \frac{1}{2\pi R_D C_D}.$$

The circuit of Fig. 14·58 (*b*) is suitable for carrier frequencies upto 100 MHz, since the usuable operational range is determined by the transconductance bandwipth of the multiplier.

In this section we have seen number of important applications of balanced modulator in communication circuits. In fact, balanced modulator, as a monolithic building block, finds wide applications in FM receivers or TV systems, and also for FM stereo decoding, colour TV chroma demodulation and video detection.

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$\frac{i^2c^2 - IPA}{L(4) - L(5)}$

Specifications of Typical IC analog multipliers

	i 8013	XR-2208	AD 531
1. Multiplier erro :	2% F.S.	0.8% F.S.	± 0.5% F.S.
2. X-nonlinearity : at V_x = 20 V ptp; V_y = ± 10 Vdc	±0.8%	0.5%	± 0.3%
3. Y-nonlinearity at V_y = 20V ptp, V_x = ± 10Vdc	±0.3%	0.5%	± 0.2%
4. ^-feed through at V_y = 0, V_x = 20 V ptp at 50 Hz.	200 mv (ptp)	120 mv)ptp)	40 mv (ptp)
5. V - feedthrough at V_x = 0, V_y = 20 V ptp at 50 Hz.	150 mv (Ptp)	120 mv)(ptp)	30 mv (ptp)
6. Small signal BW :	1 MHZ	8 MHZ	1 MHZ
7. Full power BW :	750 KHZ	-	750 KHZ
8. Slew rate :	45 V/µsec	-	45 v/µsec

E

ORDERING INFORMATION

Device	Temperature Range	Package
MC1494L	0°C to +70°C	Ceramic DIP
MC1594L	−55°C to +125°C	Ceramic DIP

MC1494L
MC1594L

Specifications and Applications Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER

. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

- Operates With ±15 V Supplies
- Excellent Linearity — Maximum Error (X or Y): ± 0.5% (MC1594)
  ± 1.0% (MC1494)
- Wide Input Voltage Range — ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small Signal) — 1.0 MHz
- Power Supply Sensitivity — 30 mV/V typical

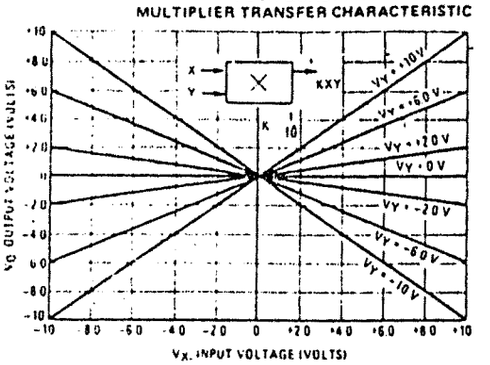
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

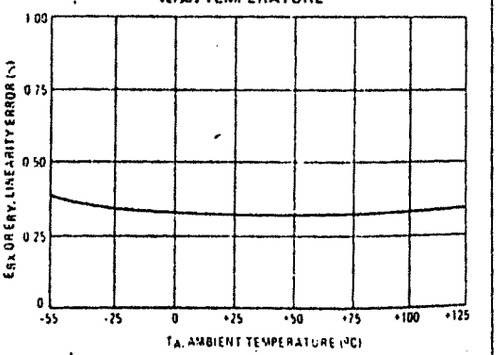
(top view)

CERAMIC PACKAGE
CASE 620

FOUR QUADRANT
MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR
versus TEMPERATURE



CONTENTS

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_8-V_6 $V_{10}-V_{13}$	$\pm [6 + (I_1 R_Y)] < 30$ $\pm [6 + (I_1 R_X)] < 30$	Vdc
Common-Mode Input Voltage $V_{CMY} = V_8 = V_6$ $V_{CMX} = V_{10} = V_{13}$	 V_{CMY} V_{CMX}	 ±11.5 ±11.5	Vdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 750 5.0	 mW mW/°C
Operating Temperature Range MC1594 MC1494	T_A	 -55 to +125 0 to + 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 V, V^- = -15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

Characteristic	Fig.	Symbol	MC1594 Min	MC1594 Typ	MC1594 Max	MC1494 Min	MC1494 Typ	MC1494 Max	Unit
Linearity Output error in Percent of full scale -10 V ≤ V_X ≤ +10 V (V_Y = ±10 V) -10 V ≤ V_Y ≤ +10 V (V_X = ±10 V) T_A = +25°C T_A = T_{high} ① T_A = T_{low} ②	1	E_{RX} or E_{RY}	 – – –	 ±0.3 – –	 ±0.5 ±0.8 ±0.8	 – – –	 ±0.5 – –	 ±1.0 ±1.3 ±1.3	%
Input Voltage Range (V_X = V_Y = V_{inp}) Resistance (X or Y input) Offset Voltage (X input) (Note 1) (Y input) (Note 1) Bias Current (X or Y input) Offset Current (X or Y input)	2,3,4	V_{in} R_{in} $\lvert V_{iox}\rvert$ $\lvert V_{ioy}\rvert$ I_b $\lvert I_{io}\rvert$	±10 – – – – –	 300 0.1 0.4 0.5 2.8	 – 1.6 1.6 1.5 150	±10 – – – – –	 300 0.2 0.8 1.0 50	 – 2.5 2.5 2.5 400	V_{pk} MΩ V µA nA
Output Voltage Swing Capability Impedance Offset Voltage (Note 1) Offset Current (Note 1)	3,4	V_o R_o $\lvert V_{oo}\rvert$ $\lvert I_{oo}\rvert$	±10 – – –	 850 0.8 1.7	 – 1.6 3.4	±10 – – –	 850 1.2 2.5	 – 2.5 5.2	V_{pk} kΩ V µA
Temperature Stability (Drift) T_A = T_{high} to T_{low} Output Offset (X = 0, Y = 0) Voltage Current X Input Offset (Y = 0) Y Input Offset (X = 0) Scale Factor Total dc Accuracy Drift (X = 10, Y = 10)		$\lvert TCV_{oo}\rvert$ $\lvert TCI_{oo}\rvert$ $\lvert TCV_{iox}\rvert$ $\lvert TCV_{ioy}\rvert$ $\lvert TCK\rvert$ $\lvert TCE\rvert$	– – – – – –	1.3 27 0.3 1.5 0.07 0.09	– – – – – –	– – – – – –	1.3 27 0.3 1.5 0.07 0.09	– – – – – –	µV/°C nA/°C µV/°C %/°C
Dynamic Response Small Signal (3 dB) X Y Power Bandwidth (47 kΩ) 3° Relative Phase Shift 1% Absolute Error	5	$BW_{3dB(X)}$ $BW_{3dB(Y)}$ P_{BW} f_ϕ f_ϵ	– – – – –	0.8 1.0 440 240 30	– – – – –	– – – – –	0.8 1.0 440 240 30	– – – – –	MHz kHz
Common Mode Input Swing (X or Y) Gain (X or Y)	6	CMV A_{CM}	±10.5 –	 -65	 –	±10.5 –	 -65	 –	V_{pk} dB
Power Supply Current Quiescent Power Dissipation Sensitivity	7	I_d^+ I_d^- P_d S^+ S^-	– – – – –	6.0 6.5 185 13 30	9.0 9.0 260 50 100	– – – – –	6.0 6.5 185 13 30	12 12 350 100 200	mAdc mW mV/V
Regulated Offset Adjust Voltages Positive Negative Temperature Coefficient (V_R^+ or V_R^-) Power Supply Sensitivity (V_R^+ or V_R^-)	7	V_R^+ V_R^- TCV_R S_R^+, S_R^-	+3.5 -3.5 – –	+4.3 -4.3 0.03 0.6	+5.0 -5.0 – –	+3.5 -4.3 – –	+4.3 -4.3 0.03 0.6	+5.0 -5.0 – –	Vdc mV/°C mV/V

Note 1 Offsets can be adjusted to zero with external potentiometers

① T_{high} = +125°C for MC1594, +70°C for MC1494 ② T_{low} = -55°C for MC1594, 0°C for MC1494

TEST CIRCUITS

FIGURE 1 – LINEARITY

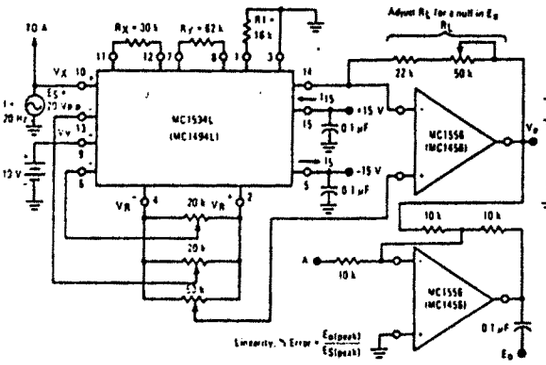


FIGURE 2 – INPUT RESISTANCE

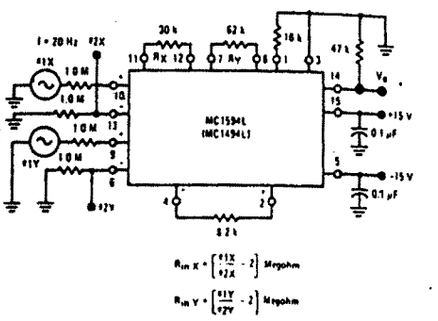


FIGURE 3 – OFFSET VOLTAGES, GAIN

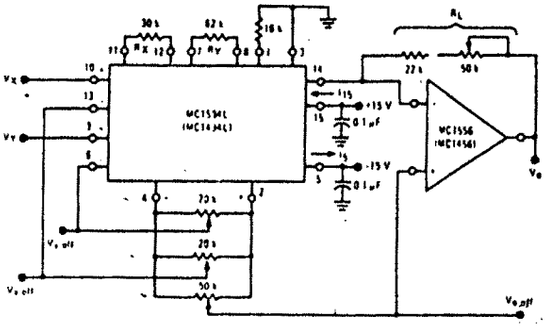


FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

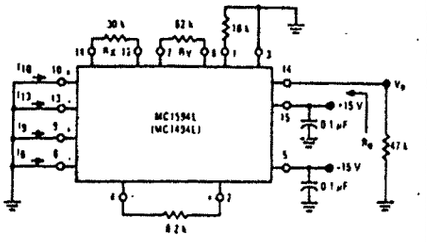


FIGURE 5 – FREQUENCY RESPONSE

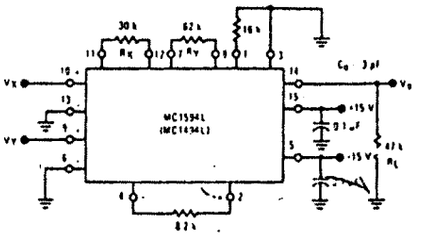


FIGURE 6 – COMMON MODE

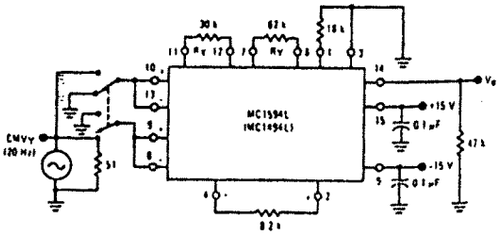


FIGURE 7 – POWER-SUPPLY SENSITIVITY

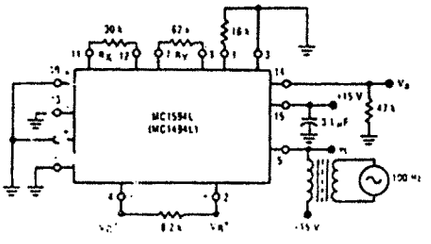
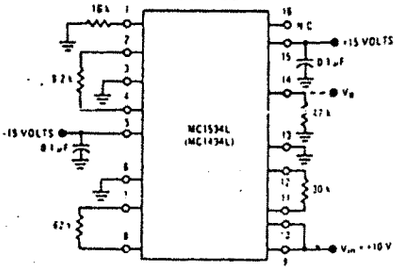


FIGURE 8 – BURN-IN



TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15$ V, $V^- = -15$ V, R1 = 16 kΩ, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, $R_L = 47$ kΩ, $T_A = +25^\circ C$)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

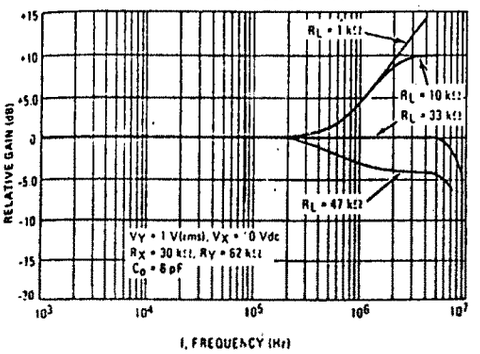


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

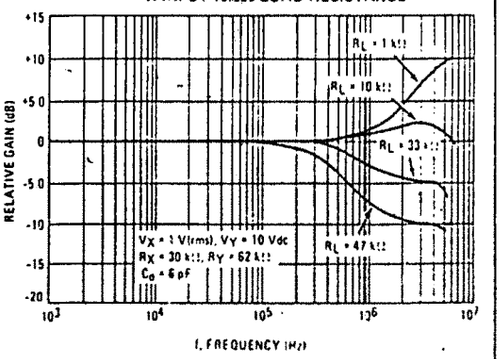


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

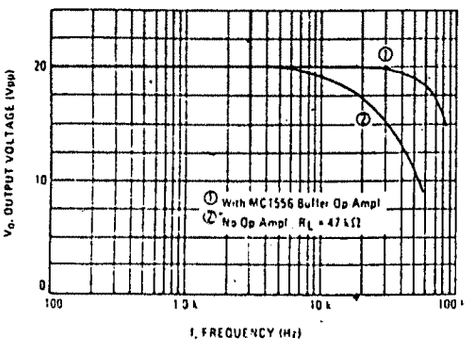


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH K = 1/10

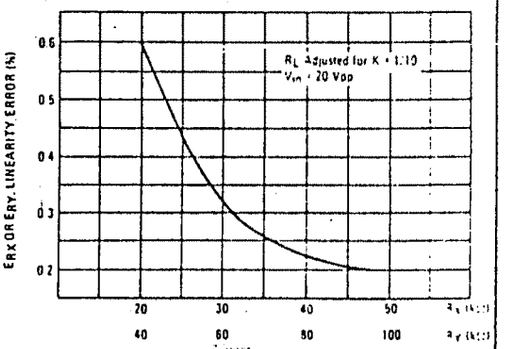


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH K = 1

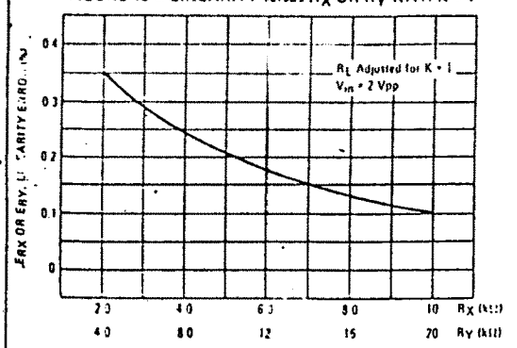
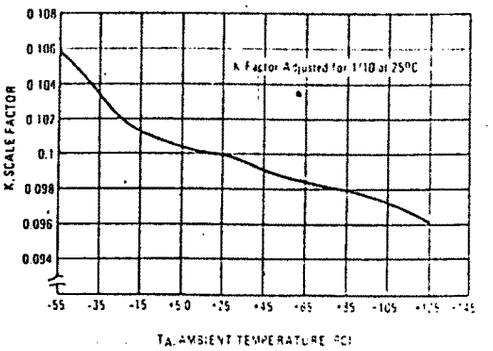


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



GENERAL INFORMATION

1. CIRCUIT DESCRIPTION

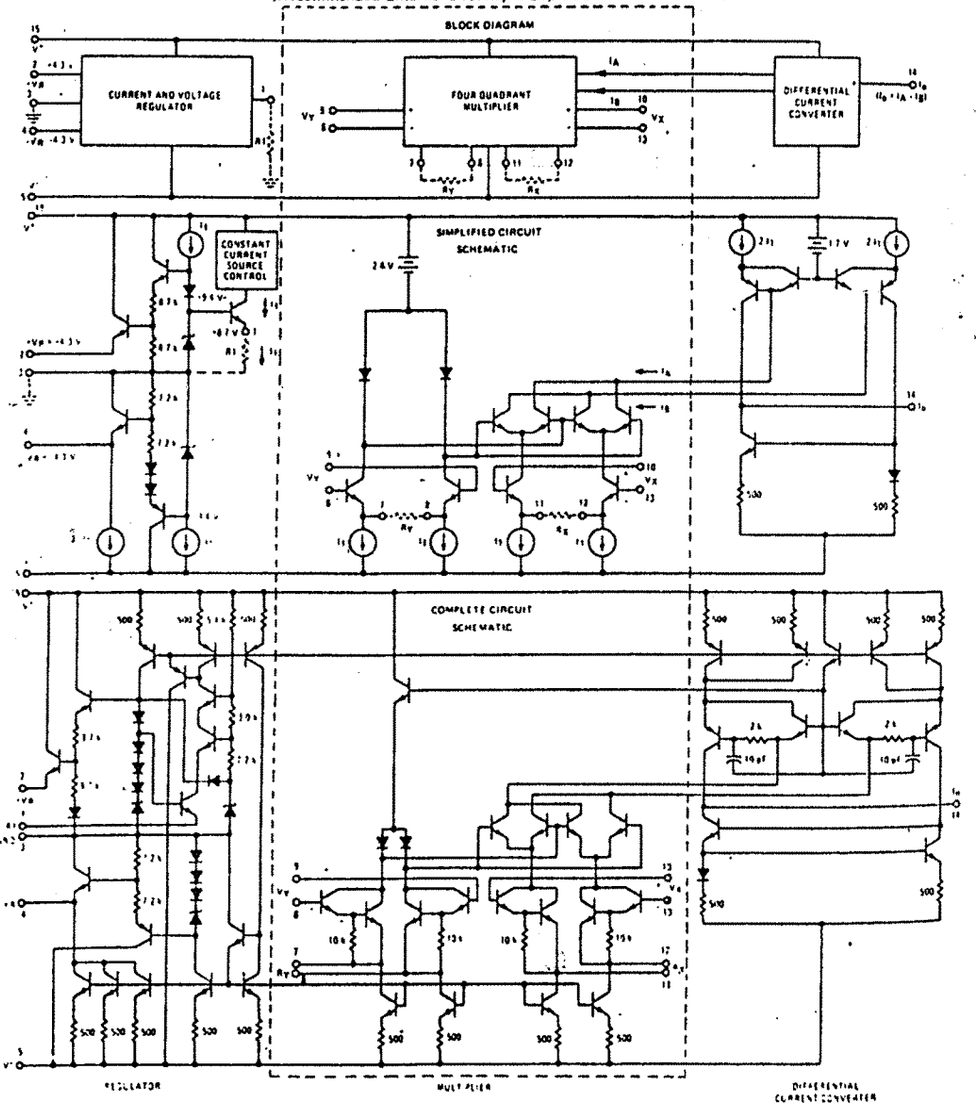
1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15

(Recommended External Circuitry is Depicted With Dotted Lines)



1.2 **Regulator (Figure 15)**

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

1.3 **Multiplier (Figure 15)**

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

1.4 **Differential Current Converter (Figure 15)**

This portion of the circuitry converts the differential output current (I_A-I_B) of the multiplier to a single-ended output current (I_o):

$$I_o = I_A - I_B$$

or

$$I_o = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_o = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = KV_X V_Y$$

where K (scale factor) = $\frac{2R_L}{R_X R_Y I_1}$

2. DC OPERATION

2.1 **Selection of External Components**

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, R_X = 30 kΩ, R_Y = 62 kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be:

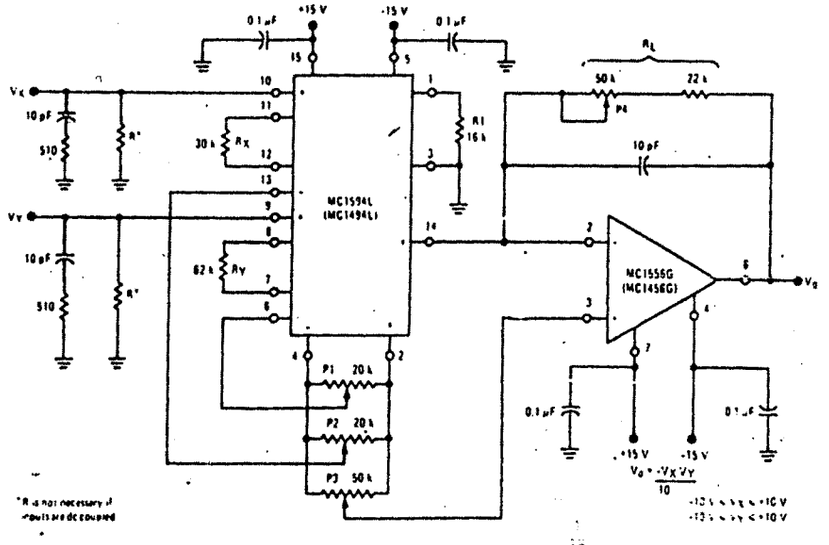
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

or $$R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$$R_X \geq 3\ V_X \text{ (max) in k}\Omega \text{ when } V_X \text{ is in volts}$$

$$R_Y \geq 6\ V_Y \text{ (max) in k}\Omega \text{ when } V_Y \text{ is in volts}$$

For example, if the maximum input on the "X" side is ±1 volt, resistor R_X can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor R_Y can be selected to be 6 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op ampl will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
   (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
   (b) connect "X" input (pin 10) to ground
   (c) adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset
   (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
   (b) connect "Y" input (pin 9) to ground
   (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset
   (a) connect both "X" and "Y" inputs to ground
   (b) adjust output offset potentiometer, P3, until the output voltage V_o, is zero volts dc

D. Scale Factor
   (a) apply +10 Vdc to both the "X" and "Y" inputs
   (b) adjust P4 to achieve -10.00 V at the output
   (c) apply -10 Vdc to both "X" and "Y" inputs and check for V_o = -10.00 V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y, and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current ($\approx 0.5\ \mu A$) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network

is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

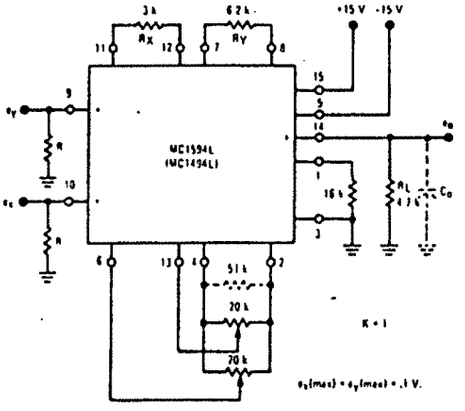
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17

FIGURE 17 – WIDEBAND MULTIPLIER



shows a typical ac multiplier circuit with a scale factor K ≈ 1. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 μA and 35 μA maximum. Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_o) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications: (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_o) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate} \quad \frac{\Delta V_o}{\Delta T} = \frac{I_o}{C}$$

Thus, if C_o is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_o}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 \text{ V/μs}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector

error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \angle 0^{o}$$

and the "Y" input is described as

$$Y = B \angle 0^{o}$$

then the output product would be expected to be

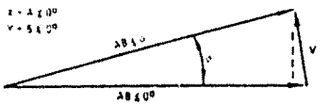
$$V_o = AB \angle 0^{o} \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \angle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



3.5 Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

4. DC APPLICATIONS

4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

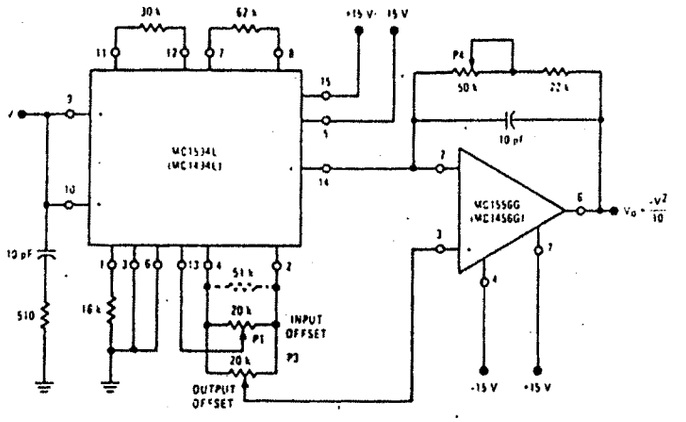
$$V_o = KV_x^2 + KV_x(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_x is determined by the internal offset, V_{iox}, but ϵ_y is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{oo} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure.

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain. (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 – MC1594 SQUARING CIRCUIT



B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_O = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10V$ Repeat steps 1 through 4 as necessary.

4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable. Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ±10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Maintain V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P1) until $V_O = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily -10 volts) constant value as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_O is -10 volts as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 20 – BASIC DIVIDE CIRCUIT USING MULTIPLIER

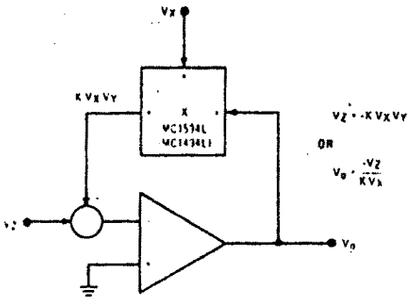


FIGURE 21 – PRACTICAL DIVIDE CIRCUIT

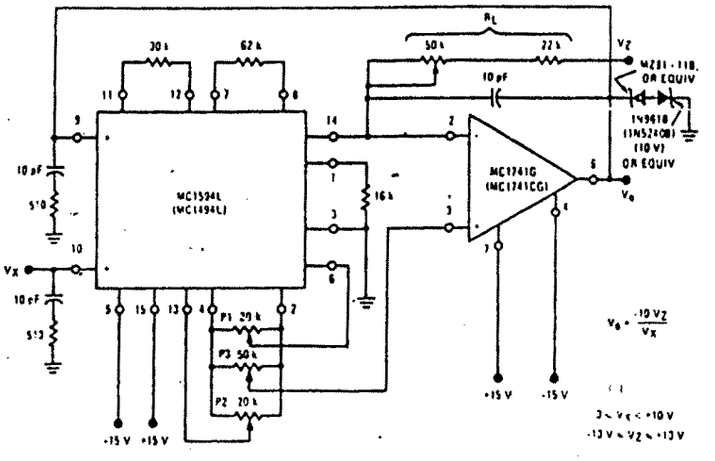
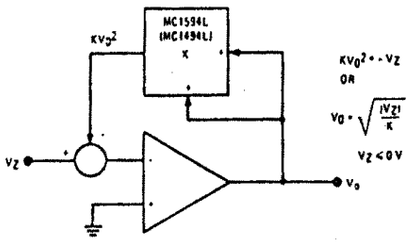


FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode.

1. Set V_Z = -0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3 Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_O to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

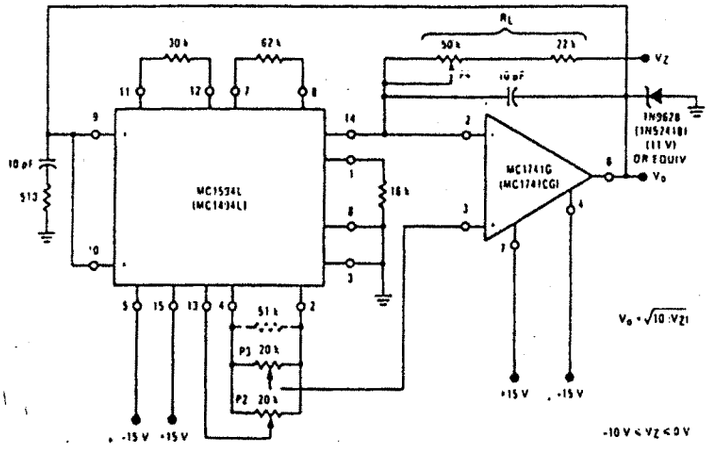
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

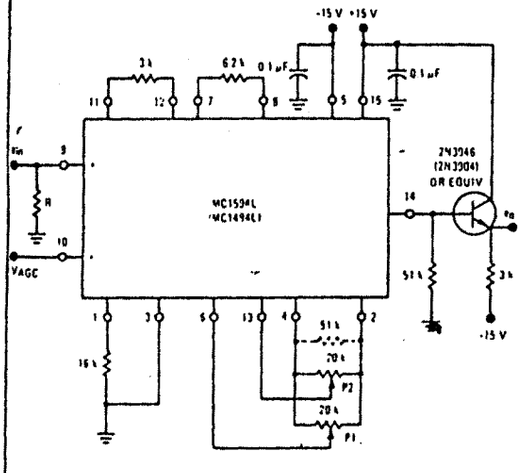
$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC

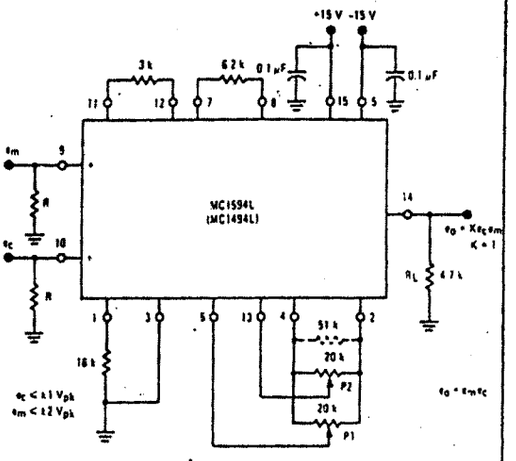


Notice that the resistor values for R_X, R_Y, and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2\cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modu-

lation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)(E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o (1 + M \cos\omega_c t) \cos\omega_c t$$

where $E_o = EE_c$

and $M = \frac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or $$e_o = \frac{E_c E_m}{2} [\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation.

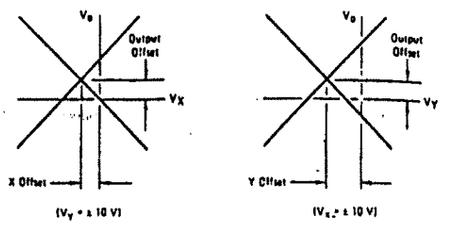
$$V_o = K(V_x \pm V_{iox} - V_{x\,off})(V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "x" input offset adjust voltage
V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



(V_Y = ± 10 V) (V_X = ± 10 V)

6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_X and V_Y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)(10 \text{ volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K(0 \pm V_{iox} - V_{x\,off})(\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$.

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is:

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y \gg \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_O = \pm[K \pm K\,(TCK)\,(\Delta T)]\,[\,(TCV_{iox})\,(\Delta T)\,]\,[\,(TCV_{ioy})\,(\Delta T)\,] \pm (TCV_{oo})\,(\Delta T)$$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at $T_A = +25^oC$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25^oC$, then:

$$V_O = [K \pm K\,(TCK)\,(\Delta T)\,][10 \pm (TCV_{iox})\,(\Delta T)\,][10 \pm (TCV_{ioy})\,(\Delta T)\,] \pm (TCV_{oo})\,(\Delta T)$$

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1 volt, 100 Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note output offset is adjusted to zero).

If an op-amp is used, the multiplier output becomes a virtual ground – the swing is then determined by the scale factor and the op-amp selected.

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