CHAPTER - 3

CHAPTER - 3

As discussed in chapter-1, the project aims at design of test & measurement system for the ferroelectric/piezoeletric ceramics & related compounds. In this chapter we propose to discuss hardware aspects of the autoranging resistance, capacitance, inductance & tanδ measurement systems designed. All these measurements are performed at the resolution of 4½ digits. The material is characterised by measuring these properties as a function of temperature. Owing to this a multichannel thermocouple input system is also included as a part of the overall system. This multichannel interface is interfaced to multi-range voltmeter via an instrumentation amplifier.

3.1 : DESCRIPTION OF THE SCHEMATIC

The fig.(3.1) shows a block schematic of a VLCRQ meter. To releave user from range switching, system has to have an autoranging capability, analog switches & the microcomputer interfaced to this systems, achieves this requirement. Main blocks forming the complete measurement system are (1) R-measurement block (2) V-measurement block (3) L & C measurement block (4) Function selector logic (5) Analog to digital converter (6) Microcomputer system. Let us discuss each one of the blocks in brief.

The R-measurement is carried out by passing a known value of current through an unknown resistor Rx, to be measured & then measuring the voltage developed across the Rx, which is in direct proportion to the value of Rs. This

the important requirement of this particular measurement is the design of a variable current source. The current variation capability is achieved through the analog switching logic. The autoranging facility is provided in this measurement by initially assuming the Rx to be in highest range & then dynamically changing the ranges till an appropriate range is encountered.

In voltage measurement, voltage between 4.096 mV to 4.096V could be measured directly. Autoranging capability is obtained by stepping gain of the instrumentation amplifier through corresponding autoranging logic. In voltage measurement, one of the main objective is to read the output from the thermocouple which are used to sense the temperatures at various locations in the measuring setup. The thermocouple interface is so designed that either direct or differential value of thermocouple output could be sensed.

The L & C measurement block works in the integrating mode for the capacitor & in the differential mode for the inductor. The measurement setup is discussed in detail in section-3. Here we shall summarise the capabilities of the measurement. The impedance & both reactance & tan δ, could be measured as a function of frequency from 100Hz to 10 MHz. The frequency is varied over each decade in the predefined steps through the microcomputer logic. The value of L is a direct measurand while the value of C is computed & displayed, (section3.7). This has been a most complicated block as far as its design & functioning are concerned.

Various methods of measurement have their own trade-offs & we have adopted a method suitable for the characterization of ferroelectric ceramics. This measurement is also an autoranging system.

Upon POWER-ON or RESET all the controlled words are in default state 00H. This logic protects each circuit from entering into saturation & unwanted power loss.

Now, the function-select logic is used to select the measurement of interest. Upon accepting the measurement choice, the logic switches over the required measurement. In brief, this logic functions like a channel multiplexer. In the default state ADC input is left grounded.

A high resolution ADC; IC 7109 (section-2.3.5), is used here to achieve accuracy of $4\frac{1}{2}$ digits in the measurement. This ADC produces binary output equivalent to input analog signal. As it is possible to interface it with the microcomputer by scaling the Vref. as required, multiple ranges are accommodated in the measuring system. Outputs in the binary form are converted to BCD through microcomputer interface. Additionally the device is capable of sensing the polarity of the input signal as well as the overflow condition, separately.

The system is dead without the control signals & the discussion would remain incomplete, if we do not make any note on microcomputer system. If the measurement system hardware is the skeleton, microcomputer is its soul. The microcomputer accepts the mode of measurement from the keyboard entries. It also determines various other

parameters from keyboard, e.g. initial & final frequency limits in the capacitance measurement. Upon accepting the parameters the mode of operation is initialized & the system is switched to automeasurement logic. The hardware logic concerned is discussed in the following sections, while the software logic is presented in chapter-4.

3.2 : R-MEASUREMENT SYSTEM

The circuit employs the following principle.

$$V_{Rx} = Rx \cdot I \qquad (17)$$

The system measures the resistances in seven ranges from 4Ω to 4 MΩ. The full range voltage developed across Rx is mapped either to 4.096 V or to 409.6 mV. Therefore the value of current in each range of R-measurement is different & maps the voltage developed to the ranges mentioned above. Table (3.2a) gives the full scale voltage, the standard current for all the ranges of measurement. Therefore aim of the circuit design is to have a switchable current source, which would source the desired current in every range of operation. This has been achieved using the following blocks (1) Reference voltage generator (2) Switchable V to I converter (3) Instrumentation amplifier. The fig.(3.2b) shows the circuit schematic.

(1) IC μA 723 has been used as a constant voltage regulator, in a constant current limiting mode. It is used as a low voltage regulator designed to provide a constant voltage of +5V. As stability of the voltage source is very important in R-measurement IC 723 proves to be the best

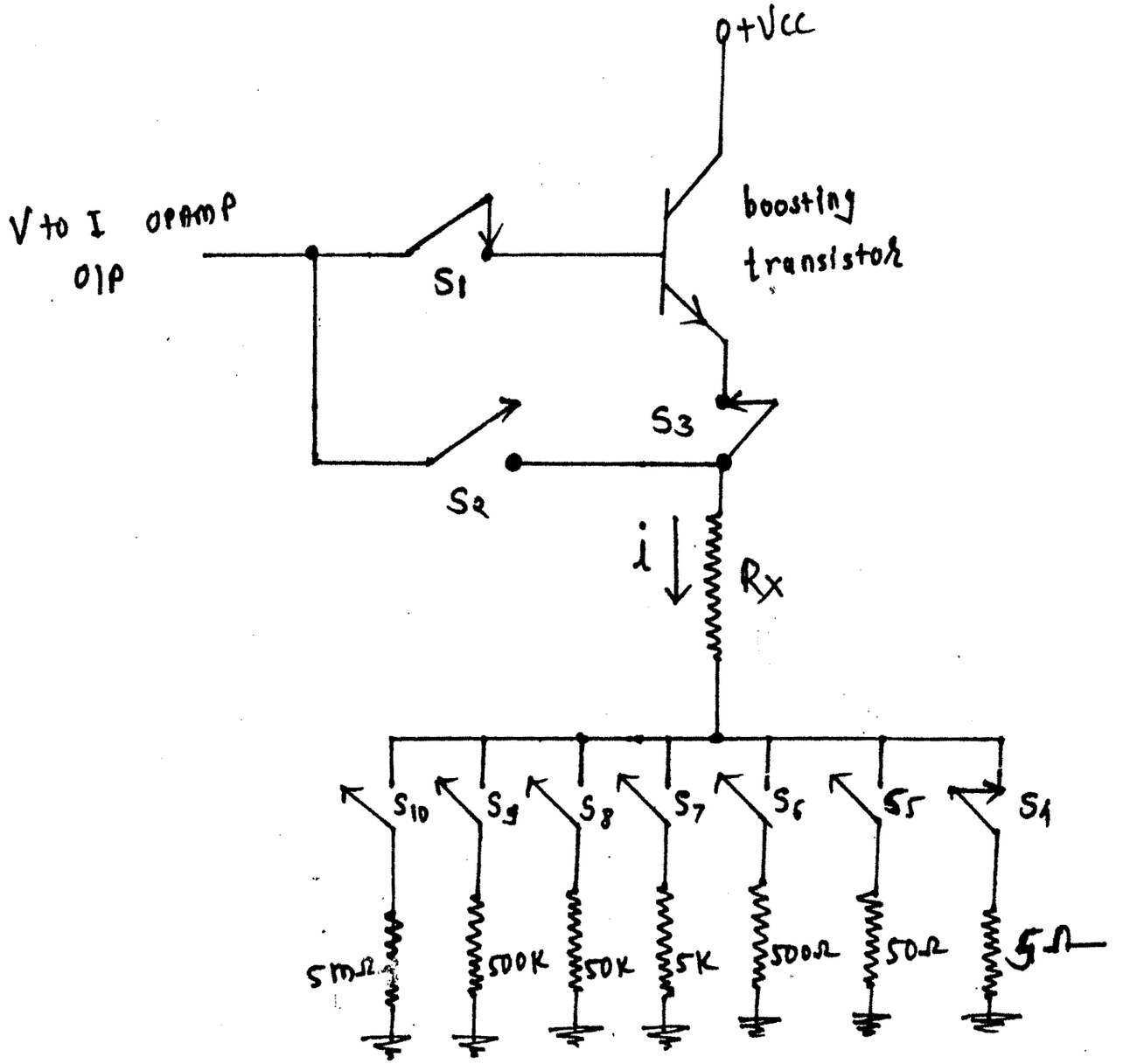


fig-3.2(1

Variable V/I Switching ckt.

R-measurement

Table No: 3.2a

SHUNT R	Rx	Iconst.	Vref.	Range
5MΩ	4MΩ	1μA	2V	00
500KΩ	400KΩ	10μA	2V	01
50KΩ	40KΩ	100μA	2V	02
5KΩ	4KΩ	1mA	2V	03
500Ω	400Ω	1mA	200mV	04
50Ω	40Ω	10mA	200mV	05
5Ω	4Ω	100mA	200mV	06

R-measurement

Table No: 3.2b

Control Bits (V-latch)								Rx	Vref.	Control Word	Range
D7	D6	D5	D4	D3	D2	D1	D0				
0	0	0	0	0	0	0	0	4MΩ	2V	OOH	00
0	0	0	0	0	0	0	1	400KΩ	2V	O1H	01
0	0	0	0	0	0	1	0	40KΩ	2V	O2H	02
0	0	0	0	1	1	0	0	4KΩ	2V	OCH	03
0	0	0	0	0	1	0	1	400KΩ	200mV	O5H	04
0	0	0	0	0	1	1	0	40Ω	200mV	O6H	05
0	0	0	0	0	1	1	1	4KΩ	200mV	O7H	06

choice which provide better linearity, higher accuracy over a wide temperature & power supply range. The design aspects of IC 723 are enclosed in the Appendix-B.

(2) Switchable V to I converter

Referring to table (3.2a) the currents to be switched range between 1μA to 100 mA. The table(3.2a) also gives the maximum power dissipated in the Rx in each range. The fixed reference of +5V is used for all these ranges of current. The basic circuit is as discussed in section 2. It is a floating load constant current source configuration. In this case the value of current is determined by the resistance shunted to ground from the inverting terminal. An analog demutiplexer IC(No.6) shunts the demultiplexer resistances from 5Ω to 5MΩ to provide the currents as in table (3.2a). The values of these resistances are also indicated in the table.

The basic V to I converter used is LM 301 with output limited to +5 volts max.(section2.3.9). Referring to appendix B the Io max of LM301 is 10 MA. Therefore for the current ranges of 100 mA the current source configuration used is floating load with binolar transistor (sec.2.3.9). The analog switches IC (No.4&5) selects the current boosting transistor for the resistance range of 4Ω full scale. The switching logic is shown in fig.(3.2a). The control inputs O1, O2, O3 of R-latch are used to multiplex the current while O4 & O3 are used to control the reference voltage of ADC. The control words corresponding to R-latch for the resistance ranges are given in table (3.2b). The reference

voltage of ADC is also indicated in the table. Upon power ON or RESET the R-latch will be at 00H. This is the range which corresponds to 4MΩ (table 3.2b). This assures the correct working of autoranging logic described in chapter-4.

In the R-measurement, the value of Rx has no effect on the constant current value, i.e. Rx can be varied without affecting the current with the assumption that the regulator voltage is constant viz. in the earlier paragraphs we have made more emphasis on the stability of the voltage source. For the lower values of Rx, stability of the voltage source is not critical since the current requirements are quite large. But for higher values of Rx for e.g. 4MΩ the current requirement reduces to 1μA & here the stability of the voltage source plays its role. Even the slightest change in current changes the measurand value drastically. From the table it is apparent that for the lower ranges of Rx measurement the reference is switched to lower value mainly to avoid excess current demand from the current source. Autoranging capability is achieved by sensing the overflow output from the ADC & comparing it with the reference value. If the value of Rx is greater than 4MΩ, it will indicate overrange but it cannot detect the short-circuit condition.

(3) Instrumentation amplifier :

Features of instrumentation amplifier are already discussed in section (2.3.3). The ckt in fig. uses LF357A for its virtue of low bias current. The minimum current that would flow through Rx is 1 μA, in the measurement range of 4MΩ. Therefore the bias current of the amplifier IC has

to be less than 1nA. The LF357A is a MOSFET input OPAMP designed to provide high input impedance ($Ri>10^{12}\Omega$) & it has the bias currents of 30pA. Gain of the amplifier in this case is adjusted to unity. The d.c level & common mode null adjustments are also incorporated in the circuit. This is a standard configuration discussed by (ref.6.1). Output of the amplifier is coupled to ADC via function selector logic.

As mentioned in earlier paragraphs O_3 & O_4 control inputs from R-latch are Ex-ORed so that if the o/p of Ex-OR gate is high it selects a reference voltage of 2V for the ADC & if the o/p is low it selects a reference voltage of 200 mv for the ADC.

3.3 : V-MEASUREMENT SYSTEM

The V-measurement system is primarily designed for measuring the thermocouple voltages but external d.c. voltages upto ± 4.096 volts could also be measured directly. The measurement voltage input can be tailored to accept voltages of higher values than that of ± 4.096 volts by attaching an input attenuator network. to the V-measurement system. The fig. shows a V-measurement system containing an instrumentation amplifier (I.A) with variable gain. The gain of the I.A. can be varied by varying a single resistor `r', as shown in fig.[3.2b] by the formula -

$$\frac{Vo}{V2-V1} = \left(1+\frac{2R1}{r}\right) \qquad (17)$$

This has been made use of for switching the gain of I.A. from one value to another using the analog switching

Function - Selection :

Table : 3.1

Control Bits								Function Selected	Control Word
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	NONE	OOH
0	0	0	0	0	0	0	1	R	O1H
0	0	0	0	0	0	1	0	V	O2H
0	0	0	0	0	0	1	1	C/L	O3H
0	0	0	0	0	1	0	0	Tanδ	O4H

$V_{measurement}$

Table :3.3

Control Bits (V-latch)								Gain	Vref.	Control Word	Range
D7	D6	D5	D4	D3	D2	D1	D0				
0	0	0	0	0	0	0	0	1	2V	OOH	00
0	0	0	0	0	1	0	1	1	200mV	O5H	01
0	0	0	0	0	1	1	0	10	200mV	O6H	02
0	0	0	0	0	1	1	1	100	200mV	O7H	03

IC(13). Refer to table (3.3) for control word to change the gain. The table clearly shows that for the measurement range of 4V & 400 mV the gain of the I.A. is unity. The ADC is selected for the reference voltage of 2V, for the input voltage range of 4V, while for the ranges. 400 mV, 40mV & 4 mV the ADC operates with referens voltage of 200 mV. To map the voltage input to ADC to 400 mV full scale, the gain of the instrumentation amplifier is set to 10 & 100 for the measurement ranes of 40 mV & 4 mV respectively.

The dot logic of the display switches the dot point correctly to display the exact value of the input voltage. The dot logic & unit display are the dedicated tasks of the microcomputer. The gain control word is sent by the microcomputer system to the V-latch. The control signals are connected to the A,B,C inputs of an analog switch, which then selects the gain of the I.A. The difference input of an I.A. is converted to the single ended o/p which can be directly connected to the analog input of ADC. As the circuit is designed to measure 4 mV input in $4\frac{1}{2}$ digit display form, the least count of the meter is 1 μV. The polarity of the input voltage does not matter since the ADC 7109 is capable of detecting the polarity of the input voltage & avails the user with polarity output signal, which is used to indicate the polarity of the i/p. The polarity flag is connected to an LED display via a buffer to indicate the polarity. This procedure is adopted, as the standard $\frac{1}{2}$ digit display is meant to display ± 1 only. The present circuit configuration works till ± 4, as its most

significant BCD. This part is further discussed in sec.(3.6) It is to be noted further that the input impedance of the voltmeter is more than $10^{12}\Omega$ as LF357A Opamps form the input stage of the I.A.

Similar to the other measurements, autoranging facility is provided for this measurement also. For autoranging, it initially assumes the maximum range for an input voltage & hence selects the unity gain for an I.A. The range is changed if the input signal is below 400 mV or 40 mv or 4 mv. In this measurement too, the overflow flag is sensed & the correct action is initialised. The necessary dot point logic & unit are displayed along with the answer. If the input voltage exceeds the voltage allowed for maximum range, overrange is displayed.

An shown in the circuit diagram in fig.(3.3), the 3rd & 4th LSBs are connected to an exclusive OR gate whose output selects the ADC reference. If the output is high, it selects 2 V reference while if the output is low, it selects 200mV reference.

3.4 : MULTICHANNEL THERMOCOUPLE INPUT SYSTEM

As far as low temperature range of measurement is concerned, the thermal equilibrium plays a dominant role. The sample and its environment is many times required to attain isothermal conditions before a measurement sequence is initial. For this purpose not only temperature at various nodes are sufficient, but temperature difference between two nodes is very important. We deviced an analog

switch interface where four thermocouples could be connected & microcomputer may select any one of these as required. Further the switching logic allows direct measurement of difference between two thermocouple outputs also. For this purpose the concerned thermocouples will work as the differential thermocouples. The thermocouples are marked as TC1, TC2, TC3, & TC4,. The differential thermocouples will be TC1-2, TC1-3, TC1-4, TC2-3, TC2-4 & TC3-4. We also allow combinations TC2-1, TC3-1, TC4-1, TC3-2, TC4-3, as separately switched inputs.

It can be seen from the circuit diagram that five analog switches are used to provide various modes for the multichannel thermocouple system. In one mode it selects the differential i/p i.e. two thermocouples with their positive ends connected to I.A & negative ends grounded, are selected. In the other mode any one of the thermocouples could be selected with its +ve & -ve ends connected to I.A. Table.3.4 shows the control word format for TC selection. The two bits M & INH are the control bits for the analog switches. Of which switch-1 (IC12) is always selected for any mode while the other switches are selected by the mode set bit M & inhibit bit INH. Upon reset both the bits are reset. As shown in the circuit diagram. These two bits are connected as inputs to the first NAND gate. When both the inputs are low, the output of the gate 1 is high, which is connected to the active low enable input of analog switch IC(14) thereby disabling switch (5). The gate-2 is connected as an inverter. So the high output of gate-1 is

TC Selection Control word Format

Table : 3.4

Control Bits (TC-select latch)								TC Combination	Control Word
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	b1	b0	a1	a0	M	INH		
0	0	0	0	0	0	0	0	1-1	OOH(Reset)
0	0	0	0	0	0	1	1	1	O3H
0	0	0	0	0	1	1	1	2	O7H
0	0	0	0	1	0	1	1	3	OBH
0	0	0	0	1	1	1	1	4	OFH
0	0	0	1	0	0	0	1	1-2	11H
0	0	1	0	0	0	0	1	1-3	21H
0	0	1	1	0	0	0	1	1-4	31H
0	0	0	0	0	1	0	1	2-1	(11H)
0	0	1	0	0	1	0	1	2-3	25H
0	0	1	1	0	1	0	1	2-4	35H
0	0	0	0	1	0	0	1	3-1	(21H)
0	0	0	1	1	0	0	1	3-2	(25H)
0	0	1	1	1	0	0	1	3-4	39H
0	0	0	0	1	1	0	1	4-1	(31H)
0	0	0	1	1	1	0	1	4-2	(35H)
0	0	1	0	1	1	0	1	4-3	(39H)

inverted to low at the output of the second gate, thereby enabling the switches 2,3 & 4. As mentioned earlier switch-1 is permanently selected by grounding its enable input. The switches 2 & 3 connect the negative ends of the thermocouples to the ground potential. The a_o-a_1, & bo-bl control signals are also logically low (reset condition). Therefore both the inputs of instrumentation amplifier are connected to high end of TC1, that is they are shorted. The connection of I.A. appear through analog switch 1 & 3 [IC12,15]. Thus the differential input to an I.A. is TC1-TC1 i.e. zero.

When mode bit M & INH are active high, the output of gate-1 goes low & that of gate-2 goes high. This enables analog switch-5 while disabling the analog switches 2,3 & 4. The IC selection control bits for the analog switches 1 & 5 are ao & al, while the control bits bo & bl are of the type don't care & may be assumed to be zero or active low. The control bits ao & al, determines the thermocouple selection. If both the bits are low, TC1 & TC1 from analog switches 1 & 5 get selected. So only one thermocouple gets selected at any time with its high end connected as one input to the I.A. & low and as the other input. The I.A. concerned is the V-measurement mode circuit.

In the third mode i.e. when mode bit M is set low & INH is set high, the output of gate-1 goes high, while that of gate-2 goes low, thereby enabling the analog switches 2,3 & 4, while disabling the switch-5. In this mode the TC selection is done by the control bits ao-al & bo-bl. ao-al

selects the high end of one of the four thermocouples where as bo-bl selects the high end from one of the remaining thermocouples. The low ends from all the thermocouples are grounded through the switches 2 & 4. In this particular mode it is possible to measure the difference of voltages from any two thermocouples. It will be useless to set 90-91 & bo-bl to be equal because it will do nothing but to select the same thermocouples from the analog switches 1 & 3, whose difference will be always zero.

The TC selection control word is sent by the micro computer on users demand, to the TC-select latch.

3.5 : ANALOG TO DIGITAL CONVERSION SELECTION

A 40-pin DIP ICL7109A is used for conversion purpose. It can sense the input voltages ranging from 0 to ± 5V & provides a 12-bit binary output. In addition to the binary output it provides polarity indication & overflow indication. The IC is capable of working in two different ranges viz. 0 to ± 4.096V & 0 to ± 409.6 mV [it may work with any other reference voltage between 2V to 200 mV, but these ranges directly corresponding to LSB equal to 1 mV or 100μV respectively]. Some hardware changes have to be made while we are switching from one range to the other range. The hardware changes could be made using analog switching circuits. For 200 mV reference the supply should get connected through 1K pot & 24K resistance to the reference out terminal & the variable of the 1K pot should get connected to Ref-in(+) of the ADC, as shown in the fig.3.5 &

a 20K resistance should get connected between pt.ß & BUF pin on the ADC. For the 2V reference, the connections remain unchanged while only the component values get changed i.e. instead of 1k pot & 24K resistance only 20K pot gets connected & the variable of the 20K is connected to Ref-in (+) of the ADC. Simultaneously, instead of 20K resistance, 200KΩ resistance gets connected between pt.B & BUF pin on the ADC. The selection is performed using analog switches, IC46,47 &48 in the ADC section. The switching control signal is given through a three input NOR gate. When any one of its input is high, a 2V reference is selected & if all the inputs are low, 200mV reference gets selected. The three inputs to the NOR gate are the outputs of each of the Exclusive-OR gates from the three measurement systems.

The two latches connected at the ADC output are used to read the 12-bit digital output. The lower 8-bits are read through one latch, while the upper 4-bits with polarity & overflow flags are read through the other latch. The ADC section also includes a function selector latch & the function selector multiplexer. The microcomputer sends the function selector control word to the function selector latch. These control signals are connected to the analog multiplexer, which connects the output from the selected function to the analog input of the ADC. Upon reset, none of the functions is selected & the ADC input gets connected to the ground potential via the analog multiplexer [IC49]. Thus the ADC is made capable of converting the analog input voltage from any one of the measurement systems.

3.6 : KEYBOARD AND DISPLAY SECTION

To have more friendly environment with the microcomputer & to send the message to the microcomputer, the input device like keyboard is interfaced with the microcomputer system & the result of the measurement is conveyed to the display section. Both these sections are controlled by a single dedicated chip INTEL 8279, also called "the keyboard/display controller" chip. This chip has an access to 64 key/256 key matrix, of which only 21 keys are used in our system. The chip can control maximum sixteen display units of which we have used eight display units. First four displays are used for numeric readout while the next four displays are used for the alphanumeric readout. Lines RLo-RL7 (Return lines) of the 8279 are connected to the rows of the 24-key matrix keyboard & the output lines (Ao-A3 & Bo-B3) are connected to drive the LED segments of the seven segment and fourteen segment displays through an eight input current driving IC...(ULN2003). The three scan lines are connected to the decoder, the 74LS156, to generate eight decoded signals. In this circuit all the eight output lines of the decoder [IC55] are connected as digit drivers to turn on four seven segment LED's & two alphameric LED's. In addition, the first three output lines of the decoder are also used to scan the rows of the keyboard.

If the microcomputer system has a 3.072 MHz clock, & when the 8279 is reset, the clock prescalar for 8279 is set to 31. This divides the clock frequency by 31 to provide

the scan frequency of approximately 100 KHz. The reset signal also sets the 8279 in the mode of sixteen character displays with two key lock-out keyboard mode.

The 8279 provides the display information of 8-bits. The numeric displays [FND 542] are seven-segment units with a decimal point display, thus require an 8-bit information of the display. On the other hand the alphanumeric displays used to display the symbols like milli, micro, nano, pico, kilo, mega or the units like Ω, V,F,Hz are fourteen segment units. Therefore fourteen information lines are required to display these quantities. For this purpose we have treated one alphanumeric display as combination of two seven-segment units. We are using two such displays. This is equivalent to use four seven segment display units. The scan line decoder (IC55) outputs 5 & 6 are used to enable alphanumeric display-1 while the scan line decoder (IC55) outputs 7 & 8 enable the alphanumeric display-2.

The information to be displayed on the alphanumeric displays is multiplexed in the following manner. Out of the fourteen information bits first seven are outputted when decoder line-5 (line-7) is active low, while the next seven bits of information are outputted when decoder output line-6 [line-8] is active low. The alphanumeric display is a common-cathode configuration. This means that if the information bit is equal to `1' the LED segment glows, while it does not glow if the information bit is `0'. During display of first seven bits, the next seven bits are set to zero. This is achieved by connecting an AND gate logic.

The decoder output-5 (o/p-7) enables the first set of AND gates. This displays first seven information bits. Similarly the second set is displayed using decoder o/p-8.

One more block which is included in this section is the address-selector IC53. A 4 to 16 decoder IC, the 74LS 154, is used as an address selector. It can select maximum sixteen I/O devices. As shown in the fig.3.6 address lines A10-A13 are used as the inputs of the decoder & address lines A14 & A15 are used as the enable lines for the decoder connected to É1 & É2 which are active low enable. Address line A8 is connected to Ao of the 8279. This address line selects either command mode or datamode for the 8279 (IC54). The first o/p of the decoder IC53 is used as a chip-select line for the 8279. The output of the decoder is selected by address lines A10-A13. The control word formation for the selection of the addresses of the device can be shown as, an example, below

A15	A14	A13	A12	A11	A10	A9	A8
enable signals for device selector		device selector					for 8279
0	0	0	0	0	0	X(0)	0=OOH (data mode for 8279)
0	0	0	0	0	0	0	1=01 H (command mode)

The table 4.2 shows the device selecting address.

The 8279 has to be initialized before the measurement starts. The information to be displayed is sent to the display RAM. The 8279 takes over the task of displaying the

characters by outputting these codes. To read the keyboard, the 8279 scans the columns, if a key closure is detected, it debounces the key. If a key-closure is valid, it loads the key into the FIFO. The valid key closure is indicated by 8279 in two ways; one, by setting an interrupt input & two, by setting a status flag. In our system, polling method is used. In this method the status word from 8279 is read & the valid keypress is detected. Upon finding the valid key press necessary action is initialized.

Remaining part of the microcomputer interface is very standard bus structure. At present we present the address decode table of the various latches used in the measurement system as table (4.2).

3.7 : THE CAPACITANCE MEASUREMENT

The overall circuit for the capacitance, inductance & tanδ measurement is a bit complicated, therefore initially we shall attempt to describe the C & tanδ measurement systems. Further it is to be noted that the same circuit works for impedance measurement in general. Therefore the value of the capacitance is computed by the microcomputer. Additionally as the circuit measures the impedance as a function of frequency the same circuit provides the inductance measurement also.

The actual circuit is given in, fig.3.4c. Initially we shall attempt to discuss the block schematic of the measurement circuit, fig.3.4a & understand the principle of measurement.

Table No : 3.6a

$C_{measurement}$

PERMITTIVITY	DISC. DIA in meters	DISK THICK in meters	CAPACITANCE (μF)
100	0.015	0.002	7.8263×10^{-5}
100	0.015	0.005	3.1305×10^{-5}
200	0.015	0.002	1.5652×10^{-4}
200	0.015	0.005	6.2610×10^{-5}
300	0.015	0.002	2.3478×10^{-4}
300	0.015	0.005	9.3915×10^{-5}
500	0.015	0.002	3.9131×10^{-4}
500	0.015	0.005	1.5652×10^{-4}
800	0.015	0.002	6.2610×10^{-4}
800	0.015	0.005	2.5044×10^{-4}
1000	0.015	0.002	7.8263×10^{-4}
1000	0.015	0.005	3.1305×10^{-4}
1300	0.015	0.002	1.0174×10^{-3}
1300	0.015	0.005	4.0696×10^{-4}
1800	0.015	0.002	1.4087×10^{-3}
1800	0.015	0.005	5.6349×10^{-4}
2000	0.015	0.002	1.5652×10^{-3}
2000	0.015	0.005	6.2610×10^{-4}
2500	0.015	0.002	1.9565×10^{-3}
2500	0.015	0.005	7.8263×10^{-4}
2800	0.015	0.002	2.1913×10^{-3}
2800	0.015	0.005	8.7654×10^{-4}
3000	0.015	0.002	2.3478×10^{-3}
3000	0.015	0.005	9.3915×10^{-4}

Frequency versus ImpedancE Table for various capacities :

Table : 2.1

Capacitance Frequency	40pF	400pF	4nF	40nF	400nF	4µF	40µF
100	40MΩ	40MΩ	400KΩ	40KΩ	4KΩ	400Ω	40Ω
1000Hz(1KHz)	4MΩ	400KΩ	40KΩ	4KΩ	400Ω	40Ω	4Ω
10KHz	400KΩ	40KΩ	4KΩ	400Ω	40Ω	40Ω	0.4Ω
100KHz	40KΩ	4KΩ	400Ω	40Ω	4Ω	0.4Ω	0.04Ω
1MHz	4KΩ	400Ω	40Ω	4Ω	0.4Ω	0.04Ω	0.004Ω

D/A CONTROL FORMAT TABLE : 4.4

Fcount	Fcount	Io	Io	Vo	Vo	Vy (XR-2208)	Vy (XR-205)
OOH	FFH	0	255I,	02	255I,R2	10V	OV
12H	EDH	18I	237I,	18I,R	237I,R2	9.1V	-0.6V
26H	DBH	36I1	219I,	36l,R	219I,R2	8.2V	-1.2V
36H	C9H	54I1	201I,	54I,R1	201I,R2	7.3V	-1.8V
48H	B7H	72I	183I,	73I,R1	183I,R2	6.4V	-2.4V
5AH	A5H	90I,	165I,	90I,R1	165I,R2	5.5	-3.0V
6CH	93H	108I,	147I,	108I,R1	147I,R2	4.6V	-3.6V
7EH	81H	126I,	129,	126I,R1	129I,R2	3.7V	-4.2V
90H	6FH	144I,	111I,	144I,R1	111I,R2	2.8V	-4.8V
A2H	5DH	162I,	93I,	162I,R1	93I,R2	1.9V	-5.4V
B4H	4BH	180I,	75I,	180I,R1	75I,72	1V	-6.0V

The circuit includes the following blocks. V10, integrator, phase-sensitive detector (PSD), Low-pass filter & ADC. The ADC is discussed separately in, section 3.5.

The integrated circuit XR-205 is used to generate the reference signal of desired frequency (Appendix D). Using additional instrumentation a sine wave & two square wave components are derived from the VCO. The square-wave component C is in phase with the sinusoidal component while the square-wave component B lags in phase by $\pi 2$. The sine wave output is amplified at the desired level, dependent on the frequency of the wave. The square waves are 10 volt peak to peak outputs. The outputs are level shifted to ground. The variably amplified sinusoidal output & the switchable resistance R forms a frequency dependent current source. This current is passed through the impedance under-test. The voltage developed across the impedance has the resistive & the reactive components out of phase by $\pi/2(90^\circ)$ These two components are separated by the phase-sensitive detectors. The in phase component refers to the reactance while the $\pi/2$ phase-shifted component refers to the reactance. The outputs of PSD's are low pass filtered & connected to ADC.

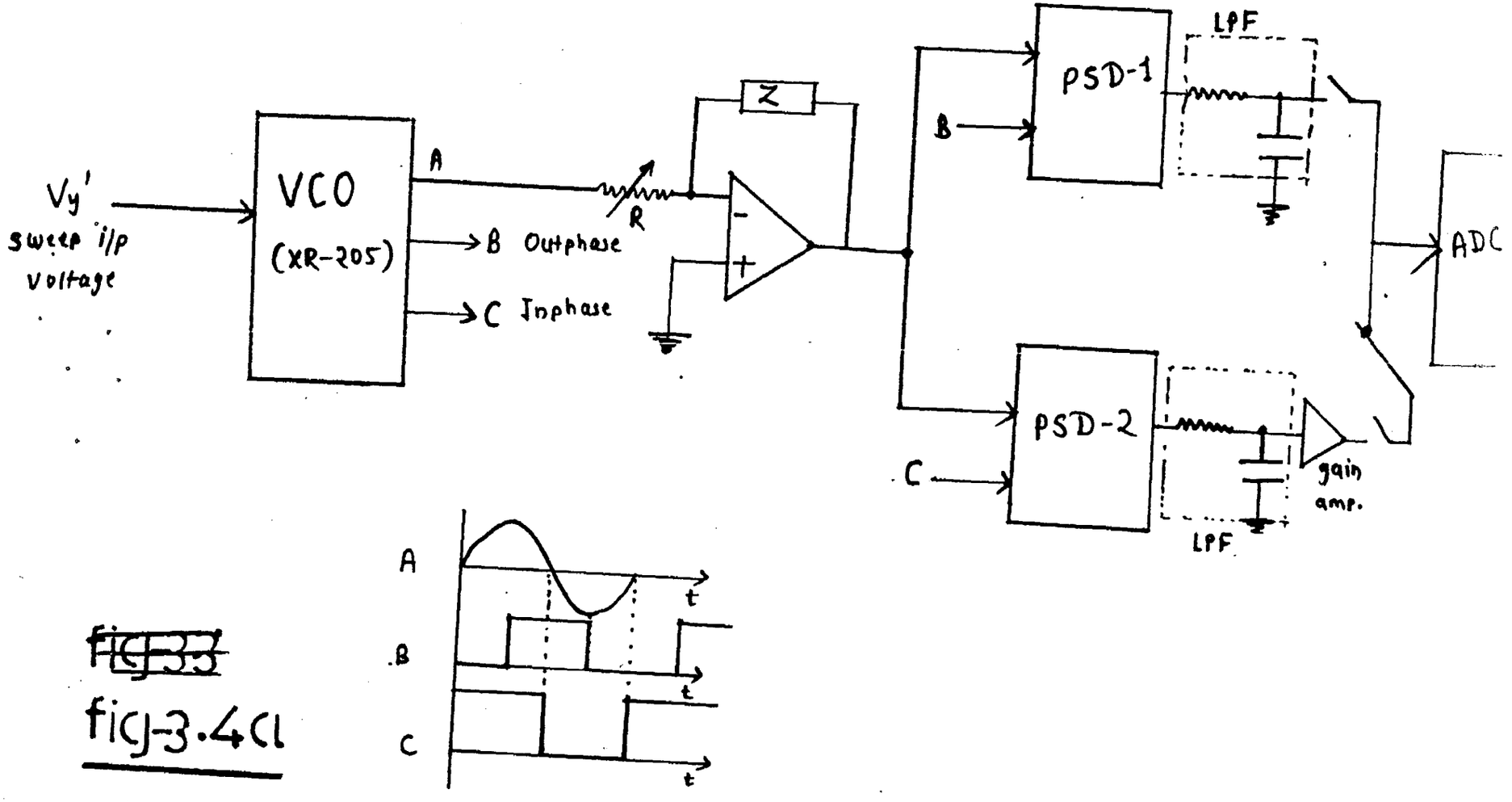
Refering to, section(2.1), it is seen that the impedance offered by a capacitor has different equational forms, dependent on whether the series or parallel equivalent circuit is suitable to represent the impedance observed. Similar is the situation for 'Z' having inductive reactance. It is a bit early to say that the system we have

Table No.: 3.6d

$C_{measurement}$

FREQ.	C	I	R	Vref./Range
100Hz	400pf	1μA	500KΩ	2V
1KHz	400pf	10μA	50KΩ	2V
10KHz	400pf	100μA	5KΩ	2V
1000KHz	400pf	1mA	500Ω	2V
1MHz	400pf	10mA	50Ω	2V
10MHz	400pf	100μA	5KΩ	200mV
100Hz	4nf	10μA	50KΩ	2V
1KHz	4nf	100μA	5KΩ	2V
10KHz	4nf	1mA	500Ω	2V
100KHz	4nf	10mA	50Ω	2V
1MHz	4nf	100μA	5KΩ	200V
10MHz	4nf	1mA	500Ω	200V
100Hz	40nf	100μA	5KΩ	2V
1KHz	40nf	1mA	500Ω	2V
10KHz	40nf	10mA	50Ω	2V
100KHz	40nf	100μA	5KΩ	200mV
1MHz	40nf	1mA	500Ω	200mV
10MHz	40nf	10mA	50Ω	200mV
100Hz	400nf	1mA	500Ω	2V
1KHz	400nf	10mA	50Ω	2V
10KHz	400nf	100μA	5KΩ	200V
100KHz	400nf	1mA	500Ω	200V
1MHz	400nf	10mA	50Ω	200mV

100Hz	4µf	10mA	50Ω	2V
1KHz	4µf	100µA	5KΩ	200mV
10KHz	4µf	1mA	500Ω	200mV
100KHz	4µF	10mA	50Ω	200mV
100Hz	40µf	100µA	5KΩ	200mV
1KHz	40µf	1mA	500Ω	200mV
10KHz	40µf	10mA	50Ω	200mV



~~fig-3.3~~

fig-3.4(1)

C-Measurement Block Diagram

developed is an impedance bridge than being a simple LCR meter. The description here next refers to capacitance represented in the series equivalent form. This has been a suitable choice for the capacitors formed out of ferroelectric ceramics (section 2.1, 2.1.1).

The series equivalent form of the capacitor is as given in fig.2C. For convenience we shall repeat the impedance & admittance equations from chapter-2.

$$Zs = \frac{RsWCs - j}{WCs}, \quad As = \frac{RsW^2C^2s + jWCs}{Rs^2W^2C^2s+1}$$

Lets us initially concentrate on the outphase component proportional to Vo(OUTphase) = Ii/W.C

$$C = \frac{Ii}{W.Voutphase} \qquad (19)$$

from this particular equations (A) it is evident that the `C' is proportional to the reciprocal of Voutphase. Two methods could be used to determine the value of C. The first method is relevant for the impedance measurement.

METHOD-1 :

Passing a known value of current `I' at frequency `W' VOUTphase is measured. I/w will be varied in each range of capacitance. The variation is I/w will be such that Vo (outphase) is in the range of reference voltage of the ADC used. In otherwords the reference voltage of the ADC determines the range of capacitance.

METHOD-2 :

The input current Ii will be increased/successive approximated such that the capacitor produces a fixed outphase. In this case the value of the input current [effectively the i/p voltage] corresponds to the value of the capacitance.

The method-1 needs the microcomputer to compute the impedance value. The microcomputer may perform the computation at a later instant of measurement. Therefore the measurement time will be determined by the ADC. On the other hand the method-2 need microcomputer to vary the input current & check the Vo to be at a required value. In this case the time of measurement will be determined by the current approximation logic. Further this method will be useful for the C-measurement in series equivalent form [or L-measurement in parallel equivalent form]. For other forms of reactances this method could not be a choice. The reason for the above argument is that the value of `C' is series combination or `L' in parallel combination is proportional to the reciprocal of Vo. The method-1 does not have any binding of this type, therefore we have adopted this method.

The selection of the input current as a function of frequency & the range of the capacitance is achieved in the following manner. The table 1/wc providing values of i/wc, as a function of frequency & selected values of `C' is repeated in this section. It is to be noted that the range of `C' will be determined by the minimum value of `C' in that range as the `Vo' is inversely proportional to `C' .

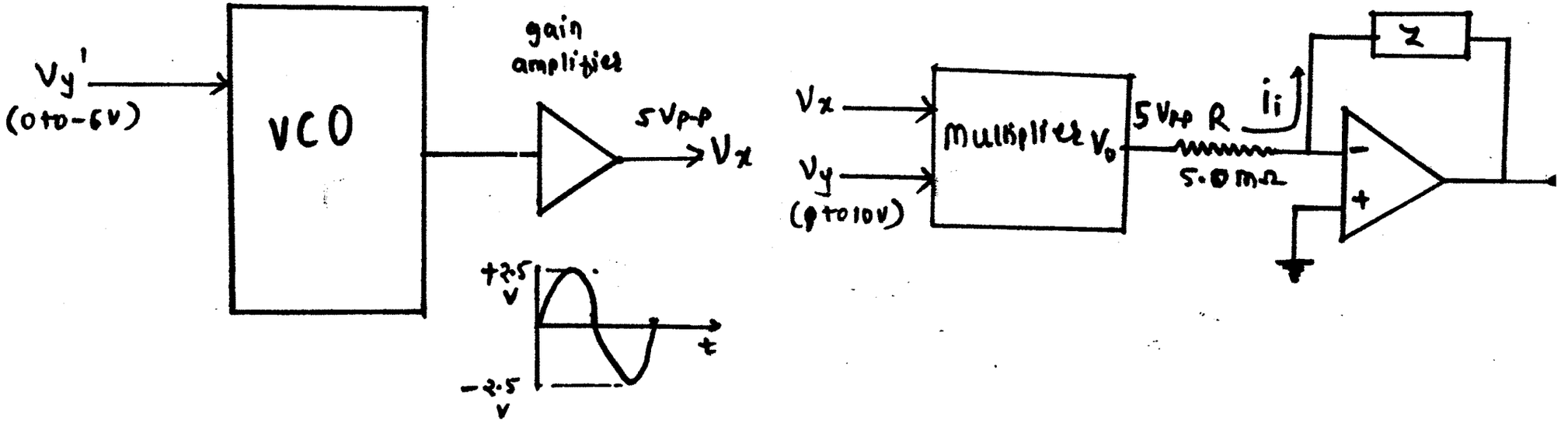


fig-3.4b

Frequency Dependent Current Sourc

The equation used to calibrate Ii is given below.

$$Ii = W.C.Vo \qquad (20)$$

In equation (20) if C is varied in a decade keeping `Ii' constant the Vo will also follow an inverse decade variation i.e. for Ii=constant at a frequency, C.Vo will also be constant. The ranges of `C' are selected such that Vomax is the reference voltage of the ADC while Vomin is 1/10th of Vomax. The resulting ranges form columns of, table 3.6d.

Now we shall take up a few examples.

e.g.(1) f=100Hz, (range=40pF to 400 pF, Vomax=4.0Volts, [In this case we desire to work in the range of Vo either at 4volts to 0.4 volts or at 400 mV to 40 mV. These values are very near to the reference voltages of ADC used].

Using equation (20)

$$Ii = 2\pi.f.C.Vo$$

$$= 2 \times 3.142 \times 100 \times 40 \times 10^{12} \times 4$$

$$= 0.1\mu A \qquad (21)$$

e.g. (2) F=1kHz, (range = 40pF to 400 pF, Vomax=4.0 volts.

$$Ii = 2. \times 3.142 \times 1 \times 10^{3} \times 40 \times 10^{12} \times 4$$

$$= 1\mu A \qquad (22)$$

From the equations 21 & 22 it is seen that as W increases by a factor of ten the reference current also increases by the same factor. Therefore for the frequencies intermediate to 100 Hz & 1kHz the reference current will be proportional to the hundred's multiple of the frequency. For further clarification the schematic of reference current generation in given in, fig.4b.

This has been an analog multiplier (XR-2208) designed to have the gain of 1/10 (ref.sec.2.3.8). Thus Vo will be equal to Vx.Vy/10. Vx is the sinusoidal input from the VCO while Vy is the control voltage which is the desired frequency multiple/fraction. The VCO XR-205 varies the output frequency over a decade. The control voltage Vy is meant to vary the frequency. It is apparent that Vy & Vy could be generated using a single control word from the microcomputer, as both these have to refer to the same frequency fraction. The values indicated in, fig.3.46 Corrosponds to the 1kHz frequency range. Vy could be used to change the frequency from 1kHz to 100 Hz. At 1kHz Vy=0, Vy=10V & Vx=5V. The input current Ii through a resistance of 5MΩ will be at 1μA as desired. Changing vy will change the frequency. Vy at V of XR205 will produce a output at 100Hz. Let U of XR-205 be at -6 volts. A digital word & a DAC could be used to generate the voltages between O to -6 volts. & the frequency output could be varied over a decade. The same digital word is used to generate Vy also. At the frequency of 100 Hz the Vy is set at 1 volts to produce the reference current of 0.1μA (refer eqn.21). Thus Vy is mapped between 10 to 1 volts & the Vy is mapped between O to -6 volts for the required frequency fractions. As discussed in later part of this section we divide each decade in the equal number of steps. Now we are again coming back to eqn(22). Now if the capacitance is increased the value of Ii will also increase, obviously at the same frequency. Now the Ii should always be such that the power

loss across the impedance is always a few milliwatts. We select 10 mA, equivalent to 40 mW of maximum power dissipation, to be the maximum current limit. Reffering to, table 3.6d.

I = 10 mA for (range =400pf = 1MHz Vref 2V)

Now if we want to go ahead for the measurements at still higher values of C, we will select Vo max at 400 mv. The table 3.6d provides the current values at Vref. ADC equal to 200 mV.

Fig.(2.3b) shows the capacitance in the vector form. For value of C at Cmin in any range the reactance 1/wc is maximum. The tan δ in given by the equation -

$\tan\delta = A/B$

We accept tanδ to be 0.4 maximum at C equal to Cmin which corresponds to tanδ = 25°. For C equal to Cmin the reactance corresponds to 4 (ADC ref.2V). If tanδ maximum is equal to 0.4 the resistive component A will be given by the equation

$A = B.\tan\delta$ (23)

$A_{max} = 4 \times 0.4 = 1.6V$

Now we have to map 1.6 volts to map the tanδ. Therefore an additional gain of 2.5 is set on the inphase component of the PSD outupt. This will map the tanδ between 0 to 4V [than at 0 to 1.6 V]. With this addition, gain computation of tanδ from ADC value will be direct and easier.

3.7.1 : DETAILS OF CIRCUIT DESCRIPTION

We shall start describing the circuit from left to right i.e. from VCO towards the PSD's. It has been already noted that to change the frequency of VCO by 10:1, the sweep voltage should change from O to -6V. Table 4.4 shows digital count & corresponding analog voltage required for XR-205 (and also Vy-input of XR-2208). As evident from the table the count is varied between OOH (O) to B4H+ (180). If the count is varied by a unit of 14H (20), there will be ten steps between OOH & B4H. Similarly the count of OAH & 05H will correspond to twenty & forty steps. This count is referred as width decrement count, while the digital word corrosponding to frequency fraction in called as Fcount. To produce the analog voltages as determined by, Table 4.4, an 8-bit D/A converter IC...(DAC 0800) is used. The latch LS373 (IC21) holds the Fcount for the DAC (IC23), sent by the microcomputer. As shown in the circuit diagram, the 5 Kilo ohm resistances connected to Vref.(+) & Vref.(-) of the DAC provide the reference current of 2mA for the DAC. The DAC produces two output currents IOUT & I out proportional to the input digital word. These two currents are used to map the voltages for the VCO (IC27) & multiplier (IC30) after the necessary signal conditioning. Signal conditioning is provided using the quad OPAMP IC25-29 (LM324) from which the OPAMPS A & B condition current Iout & OPAMPS C & D condition current Iout. OPAM's A & C are used as current to voltage converter as well as they produce the necessary voltage gain, using R1 & R2, S0 as to map the

Fcont Versus Frange frequency Table : 3.6b

Width Count = 10

Frang/Fcount	0	1	2	3	4
00	1KHz	10KHz	100KHz	1MHz	10KHz
18	900HZ	9KHz	90KHz	900KHz	9MHz
36	800Hz	8KHz	80KHz	800KHz	8MHz
54	700Hz	7KHz	70KHz	700KHz	7MHz
72	600Hz	6KHz	60KHz	600KHz	6MHz
90	500Hz	5KHz	50KHz	500KHz	5MHz
108	400Hz	4KHz	40KHz	400KHz	4MH2
126	300Hz	3KHz	30KHz	300KHz	3MHz
144	200Hz	2KHz	20KHz	200KHz	2MHz
162	100Hz	1KHz	10KHz	100KHz	1MHz

Fcount Versus Frange frequency Table : 3.6c

Width Count = 20

Frang/Fcount	0	1		3	4
00	1kHz	10KHz	100kHz	1mHz	10KHz
09	950Hz	9.5KHz	95kHz	0.95KHz	9.5MHz
18	900Hz	9.0KHz	90kHz	0.90KHz	9.0MHz
27	850Hz	8.5KHz	85kHz	0.85KHz	8.5MHz
36	800Hz	8.0KHz	80kHz	0.75KHz	8.0MHz
45	750Hz	7.5KHz	75kHz	0.75KHz	7.5MHz
54	700Hz	7.0KHz	70kHz	0.70KHz	7.0MH2
63	650Hz	6.5KHz	65kHz	0.65KHz	6.5MHz
72	600Hz	6.0KHz	60kHz	0.60KHz	6.0MHz
81	550Hz	5.5KHz	55kHz	0.55KHz	5.5MHz
90	550Hz	5.5KHz	55kHz	0.50KHz	5.0MHz
98	450Hz	4.5KHz	45kHz	0.45MHz	4.5MHz
108	400Hz	4.0KHz	40kHz	0.40MHz	4.0MHz
117	350Hz	3.5KHz	35kHz	0.35MHz	3.5MHz
126	300Hz	3.0KHz	30kHz	0.30MHz	3.0MHz
135	250Hz	2.5KHz	25kHz	0.25MHz	2.5MHz
144	200Hz	2.0KHz	20kHz	0.20MHz	2.0MHz
153	150Hz	1.5KHz	15kHz	0.15MHz	1.5MHz
162	100Hz	1KHz	10kHz	0.10MHz	1.0MHz

correct voltage levels. OPAMP B is simply a units gain invertor while OPAMP D is a d.c level shifted OPAMP & the d.c. level shifting is required to map the control voltage for the multiplier between +1V & +10Volts, otherwise the voltage may get mapped between OV & +9V for the full scale Iout variation.

As shown in the circuit diagram the output of OPAMP B is connected to the sweep input of the VCO IC27(XR-205). For the VCO, the sweep voltage is mapped between O to -6V. At OV sweep input, the VCO generates the free running frequency determined by the external capacitor. For XR-205 the freq. sweep is in the ratio of 10:1.

For e.g. if the free running frequency selected is 1kHz at OV sweep input, it will shift to 100 Hz when the sweep input voltage sweeps to -6V i.e. in the negative direction. It is important to direct the user that XR-205 (VCO) cannot tolerate positive sweep voltages, even by mistake. To achieve greater sweeping linearity, a 1 kilo ohm resistor is connected at the sweep input of XR-205 (VCO). The XR205 is a monolithic waveform generator IC capable of generating sine, square, triangular & sawtooth waveforms of which only sine & square wave outputs are used in our measurement system. As mentioned earlier this waveform generator IC generates the free running frequency determined by the external capacitor. The free running frequency is selected by the user through the microcomputer. The microcomputer sends the control word to the latch LS373 (IC22) which in turn controls or switches the IC24 to select the correct

C-measurement

Table - 3.6e

(Control word & range selection)

Frequency	Capacitance	Current	Voltage	Resistance	Control Bits (V-latch)								Control word	Crange	Frange
					D7	D6	D5	D4	D3	D2	D1	D0			
1KHz	400pf	10μA	2V	50KΩ	0	0	1	0	0	0	0	1	21H	00	00
1KHz	4nf	10μA	2V	5KΩ	0	1	0	0	0	0	0	1	41H	01	
1KHz	40nf	1mA	2V	500Ω	0	1	1	0	0	0	0	1	61H	02	
1KHz	400nf	10mA	2V	50Ω	1	0	0	0	0	0	0	1	81H	03	
1KHz	4μf	100μA	200mV	5KΩ	0	1	0	0	1	0	0	1	49H	04	
1KHz	40uf	1mA	200mA	500Ω	0	1	1	0	1	0	0	1	69H	05	
10KHz	400pf	100μA	2V	5KΩ	0	1	0	0	0	0	1	0	42H	06	01
10KHz	4nf	1mA	2V	500Ω	0	1	1	0	0	0	1	0	62H	07	
10KHz	40nf	10mA	2V	50KΩ	1	0	0	0	0	0	1	0	82H	08	
10KHz	400pf	100μA	200mV	5KΩ	0	1	0	0	1	0	1	0	4AH	09	
10KHz	4μd	1mA	200Ω	500Ω	0	1	1	0	1	0	1	0	6AH	0A	
10KHz	40μf	10mA	200mV	50Ω	1	0	0	0	1	0	1	0	8AH	0B	
100KHz	400pf	1mA	2V	500Ω	0	1	1	0	0	0	1	1	63H	0C	02
100KHz	4nf	10mA	2V	50Ω	1	0	0	0	0	0	1	1	83H	0D	
100KHz	40nf	100μA	200mV	5KΩ	0	1	0	0	1	0	1	1	4BH	0E	
100KHz	400pf	1mA	200mV	500Ω	0	1	1	0	1	0	1	1	6BH	0F	
100KHz	4μf	10mA	200mV	50Ω	1	0	0	0	1	0	1	1	8BH	10	
1MHz	400pf	10mAA	2V	50Ω	1	0	0	0	1	1	0	0	8CH	12	03
1MHz	4nf	100μA	200mV	5KΩ	0	1	0	0	0	1	0	0	44H	13	
1MHz	40nf	1mA	200mV	500Ω	0	1	1	0	0	1	0	0	64H	14	
1MHz	400nf	10mA	200mV	50Ω	1	0	0	0	0	1	0	0	84H	15	
10MHz	400pf	100μA	200mV	5KΩ	0	1	0	0	0	1	0	1	45H	18	04
10KHz	4nf	1mA	200mV	500Ω	0	1	1	0	0	1	0	1	65H	19	
10MHz	40nf	10mA	200mV	50Ω	1	0	0	0	0	1	0	0	85H	06	12

capacitor for the desired frequency range. So, to study the nature of the impedance the user has to select a frequency decade of his interest. For the measurement of C,L & tanδ, the input waveform should be centered exactly at ground potential. This is achieved by varying the 50 kilo ohm pots connected to the pins 3 & 4 of IC...(XR-205). As table 3.6e shows the control word and the base frequency selection.

As it is seen the base frequencies of 1k, 10k, 100K & 1 MHz are selected using the control words D7, D6 & D5. This allows the frequency variation over 100Hz to 1MHz in steps as described previously.

The sinewave output from the XR-205 (IC.27) is adjusted to the level 5Vp-p & connected, as X-input, to the multiplier IC30 (XR-2208) & +1 to +10V mapped output from OPAMP D (IC29) is connected as y-input of the multiplier. The gain of the multiplier is adjusted to 0.1 using external components Rx, Ry & the OPAMP gain (the OPAMP is separately provided in the IC & could be connected in various fashions.) The output from the multiplier is given by the equation -

$$V = \frac{Vx.Vy}{10}$$

The x-input & y-input nulling for the output voltage is carried out separately by the 10k pots. The callibration for output nulling is done on trial basis until the expected output is obtained. Let us try one example. We know the X-input is fixed to 5Vp-p. Suppose Y-input is equal to +10V.

Then the multiplier output would become

$$Vo = \frac{5 \times 10}{10} = 5V$$

The multiplier has been used essentially to meet the test-current requirements, demanded by the sample impedance in the integrating mode/differentiating mode, in various frequency ranges, table 3.6d.

In the frequency range of 100Hz to 1kHz; at 1kHz the reference current required in the 40 to 400 pF range is 1μA. So a 5 megaohm resistance with the input signal of 5Vp-p meets the requirements. At 100Hz, the current requirement reduces to 0.1μA. To achieve this, two methods are possible; one, by increasing the resistance value from 5 megaohm to 50 meg ohm & second, by reducing the input voltage to 0.5V & keeping the resistance of 5 megaohm fixed. (So that the current will be equal to $0.5/5 \times 10^6 = 0.1\mu A$). In the measurement system discussed here we adopt the second method making use of the multiplier (with Y-input used as multiplying factor). For the next decade of frequency range the test current requirement for the sample impedance increase by the factor of ten. So, when the frequency is changed, the resistance value required to produce the desired reference current also changes. In other words analog switching circuitry is required. This is accomplished using the analog switching IC's 33 & 36 & providing a control word. The resistance selection logic & control words are given in table 3.6e.

To detect the inphase component & outphase component from the complex nature of the impedance under test phase-detectors are essential. Low cost monolithic phase-detectors using OPAMPS & switches could be wired. The circuit configuration may become error full as it has to maintain linearity over a wide range of frequencies. We have made use of monolithic component XR-2208, a somewhat costly analog phase detector, which has the ability to operate over the desired range of frequencies.

In the circuit IC34 & IC35 are used as the phase detecting blocks. IC34.is used to detect the inphase component, while IC35 is used to detect the outphase component. The complex component (containing inphase & outphase components) at the output of the integrator is fed as one of the inputs for each-phase detector. For the first phase-detector IC35, a square wave output in phase quadrature ($\pi/2$ to $3\pi/2$ phase) is connected as 2nd input. It is derived directly from the function generator IC27, with the amplitude of 1.2 Vp-p. The amplitude level of this component is level shifted to 10Vp-p without any negative excursion i.e. Vo between 0 to +10V. This is achieved using a Schmitt-trigger OPAMP IC32 with ± 5V output & a level shifting circuit using a high frequency switching transistor. The emitter of the switching transistor is kept at slightly negative potential of the order of 0.3 volts essentially because of the drop across the transistor in the saturation state, otherwise the excursion of the square wave component may begin at + 0.3V & and at +10V.

For the 2nd phase-detector IC34, the inphase squarewave is connected, as its 2nd input. It is derived from the sine wave output of the function generator IC27, which is fed to a Schmitt trigger circuit to convert it to a square wave of ± 5V, which is then fed to a high frequency switching transistor for level shifting. The excursions of the square-wave input are adjusted to O to + 10V.

The phase-detected output from detector 1 & 2 contain large number of high frequency components which need to be eliminated. A fourth order butterworth low pass-filter has been used in the circuit to achieve optimum efficiency while filtering. For this purpose a quad-OPAMP ICLM324 is used. So as not to exceed the voltage limit of ± 5V (rated i/p of ADC) a 5 volt zener pair is strapped at the output of PSD, before it is fed to the ADC.

As discussed earlier in this section, for the tanδ measurement an additional gain of 2.5 is required to achieve full scale output (Vomax) of 4V. So an OPAMP amplifier designed for the gain of 2.5 is used in the tanδ measurement circuit.

3.8 : THE INDUCTANCE MEASUREMENT

In this case also we are employing series equivalent circuit. We shall note the differences in the circuit operation if inductance was to be measured instead of the capacitor. The reference current equation changes in this case as the impedance offered by an inductor is

$$R_s + jW.L_s. \qquad (24)$$

Therefore Voutphase = IiW.L (25)

Instead going ahead for detailed discussion on the parallel lines of C-measurement we shall make a few qualitative remarks.

1] The minimum range at 100Hz is 40 to 400 µH. Here the required reference current at ADC reference of 200mV is 15mA.

2] The Vreference and the reference current values are found in the same way as for `C' masurement. As compared to the table of reference current for the capacitance (Table 3.6d), the reference current in this case differs in the base quantity. The multiplying factors are similar. Therefore if we change the amplitude of reference sine wave these current values could be generated. This is not a difficult task.

To measure the inductance over varying frequency the current values are higher for the lower frequencies. To be specific for 400 µH, the current at 1kHz is 160mA & at 100Hz it is 1.6Amp. This current variation is achieved by an analog multiplier in our system. Further this variation is inverse of that seen for capacitance, Table 3.6d. Therefore switching is required at this stage also. The switching will map the control voltage Vy at one volt for 1kHz to ten volts for 100Hz.

Remaining part of the measurement circuit is unaltered but the task of microcomputer changes. As far as scope of this dissertation is concerned, we have not developed the detail software for Ls measurement.

F	C	I	VO
100	4E-10	1,029571E-06	4,096
100	4E-10	1,029571E-07	.4096
100			
100	4E-09	1,02957E-05	.4096
100	4E-09	1,02957E-06	.4096
100	4E-08	1,029571E-04	4,096
100	4E-08	1,029571E-05	.4096
100	.0000004	1,029571E-03	4,096
100	.0000004	1,029571E-04	.4096
100	.000004	1,029571E-02	.4096
100	.00004	1,029571E-03	4,096
100	.00004	1,029571E-02	4,096
1000	4E-10	1,029571E-05	4,096
1000	4E-10	1,029571E-06	.4096
1000	4E-09	1,029571E-04	4,096
1000	4E-09	1,02957E-05	.4096
1000	4E-08	1,029571E-03	4,096
1000	4E-08	1,029571E-04	.4096
1000	.0000004	1,029571E-02	4,096
1000	.0000004	1,029571E-03	.4096
1000	.000004	1,029571E-02	.4096
10000	4E-10	1,029571E-04	4,096
10000	4E-10	1,029571E-05	.4096
10000	4E-09	1,029571E-03	4,096
10000	4E-09	1,029571E-04	.4096
10000	4E-08	1,029571E-02	4,096
10000	4E-08	1,029571E-03	.4096
10000	.0000004	1,029571E-02	.4096
100000	4E-10	1,029571E-03	4,096
100000	4E-10	1,029571E-04	.4096
100000	4E-09	1,029571E-02	4,096
100000	4E-09	1,029571E-03	.4096
100000	4E-08	1,029571E-02	4,096
100000	4E-10	1,029571E-02	4,096
100000	4E-10	1,029571E-03	.4096
100000	4E-09	1,029571E-02	.4096
1E+07	4E-10	1,029571-02	.4096

F	C	T	R
100	4E-10	.08	318268.6
100	4E-10	.1763	701384.6
100	4E-10	.2679	1065802
100	4E-10	.364	1448422
100	4E-10	.4663	1855108
100	4E-10	.5774	2297104
100	4E-09	.08	31826.86
100	4E-09	.1763	70138.46
100	4E-09	.2679	106580.2
100	4E-09	.364	144812.2
100	4E-09	.4663	185510.9
100	4E-09	.5774	229710.4
100	4E-08	.08	3187.686
100	4E-08	.1763	7013.845
100	4E-08	.2679	10658.02
100	4E-08	.364	14481.22
100	4E-08	.4663	18551.08
100	4E-08	.5774	22971.04
100	.0000004	.08	318.2687
100	.0000004	.1763	701.3846
100	.0000004	.2679	1065.802
100	.0000004	.364	1448.122
100	.0000004	.4663	1855.108
100	.0000004	.5774	2297.104
100	.000004	.08	31.82687
100	.000004	.1763	70.13845
100	.000004	.2679	106.5802
100	.000004	.364	144.8122
100	.000004	.4663	185.5108
100	.000004	.5774	229.7104
100	.00004	.1763	7.013846
100	.00004	.2679	10.65802
100	.00004	.364	14.48122
100	.00004	.4663	18.55109
100	.00004	.5774	22.97104
1000	4E-10	.08	31826.86
1000	4E-10	.1763	70138.45
1000	4E-10	.2679	106580.2
1000	4E-10	.364	144812.2
1000	4E-10	.4663	185510.8
1000	4E-10	.5774	229710.8
1000	4E-09	.08	3182.686
1000	4E-09	.1763	7013.845
1000	4E-09	.2679	10658.02
1000	4E-09	.364	14481.22
1000	4E-09	.4663	18551.08
1000	4E-09	.5774	22971.04
1000	4E-08	.08	318.2686
1000	4E-08	.1763	701.3845
1000	4E-08	.2679	1065.802

1000	4E-08	.364	1448.122
1000	4E-08		
1000	4E-08	.4663	1855.108
1000	4E-08	.5774	2297.104
1000	.0000004	.08	31.82686
1000	.0000004	.1763	70.13845
1000	.0000004	.2679	106.5802
1000	.0000004	.364	144.8122
1000	.0000004	.4663	185.5108
1000	.0000004	.5774	7.013845
1000	.000004	.1763	10.65802
1000	.000004	.2679	14.48122
1000	.000004	.364	18.55108
1000	.000004	.4663	18.55108
1000	.000004	.5774	22.97104
10000	4E-10	.08	3182.686
10000	4E-10	.1763	7013.845
10000	4E-10	.2679	10658.02
10000	4E-10	.364	14481.22
10000	4E-10	.4663	18551.08
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10000	4E-09	.1763	701.3845
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10000	4E-09	.364	1448.122
10000	4E-09	.4663	1855.108
10000	4E-09	.5774	2297.104
10000	4E-08	.08	31.82686
10000	4E-08	.1763	70.13845
10000	4E-08	.2679	106.5802
10000	4E-08	.364	144.8122
10000	4E-08	.4663	185.5108
10000	4E-08	.5774	229.7104
10000	.0000004	.1763	7.013845
10000	.0000004	.2679	10.65802
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10000	.0000004	.5774	22.97104
100000	4E-10	.08	318.2686
100000	4E-10	.1763	701.3845
100000	4E-10	.2679	1065.802
100000	4E-10	.364	1448.122
100000	4E-10	.4663	1855.108
100000	4E-10	.5774	2297.104
100000	4E-09	.08	31.82687
100000	4E-09	.1763	70.13845
100000	4E-09	.2679	106.5802
100000	4E-09	.364	144.8122
100000	4E-09	.4663	185.5108
100000	4E-09	.5774	229.7104
100000	4E-08	.1763	7.013845
100000	4E-08	.2679	10.65802

100000	4E-08	.364	14.48122
100000	4E-08	.4663	18.55108
100000	4E-08	.5774	22.97104
1000000	4E-10	.08	31.82686
1000000	4E-10	.1763	70.13845
1000000	4E-10	.2679	106.5802
1000000	4E-10	.364	144.8122
1000000	4E-10	.4663	185.5108
1000000	4E-10	.5774	229.7104
1000000	4E-09	.1763	7.013845
1000000	4E-09	.2679	10.65802
1000000	4E-09	.364	14.48122
1000000	4E-09	.4663	18.55108
1000000	4E-09	.5774	22.97104
1E+07	4E-10	.1763	7.013845
1E+07	4E-10	.2679	10.65802
1E+07	4E-10	.364	14.48122
1E+07	4E-10	.4663	18.55108
1E+07	4E-10	.5774	22.97104